C.P.U. EXORCISOR

PRELIMINARY USER MANUAL

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OVERVIEW

The Cinematronics C.P.U. Exorcisor

The Cinematronics Exorcisor was designed to help Test Technicians diagnose circuit faults in the main logic board, a.k.a. CPU, used in all the early Cinematronics Vector based arcade games. The Exorcisor connects to the board under test and injects digital signals into a number of circuit nodes forcing the board to operate in a stable and repeatable manner. With the board in this state the technician can diagnose many component failures by simply reading the digital signatures present on the board and comparing them to the correct signatures which are shown on the schematics. Debugging becomes a simple matter of finding the device which is causing the incorrect signature and replacing it.

Signature Analysis

From the HP Test & Measurement catalog, here's a description of Signature Analysis:

Signature analysis is a fast and accurate method of troubleshooting digital circuits. Finding faults is reduced to tracing signal flow and comparing measured signatures to printouts or computer-stored signatures. A signature is a 16 bit-cyclic redundancy code (CRC) generated for blocks of data. Instead of entire bit streams, only signatures are compared to detect errors.

HP's patented signature analysis technique enables the HP5005B or HP5006A to generate a compressed, four-digit 'fingerprint' or signature of a digital data stream at a logic node. Any fault associated with a device connected to the node will force a change in the data stream and produce an erroneous signature.

In other words, a signature is a four digit Hexadecimal representation a binary pattern measured within a 'window' defined by a START and a STOP signal. The signatures that are used as a reference were measured on a 'known-good' PC board similar to the board under test (DUT). The reference board and the DUT must be driven by identical signal patterns, or exercised, to obtain the proper results. This is just what the Exorcisor does.

Equipment Necessary

- Signature Analyzer (HP5004A, HP5006A, Atari Cat Box, etc.)
- +5 Volt DC @ 5A Power Supply or Cinematronics Power Supply
- 100 MHz or higher Oscilloscope w/probes
- 2 ½ - Digit or better Digital Multi-meter (DMM) w/leads
- 16 pin DIP Clip
- Ball Clip or E-Z Hook clip leads, various lengths
- Cinematronic CPU Schematics w/signatures

SETTING UP THE EQUIPMENT

HP5004A Self-Test

This section covers the Self-Test feature of the HP5004A. If you are using a different type of Signature Analyzer you must refer to it's user manual for the Self-test operation.

1. Remove the grabber connectors from the pod test leads, and connect the pod (START, STOP and CLOCK) leads to the matching START, STOP and CLOCK receptacles on the 5004A front panel.
2. Connect the 5004A data probe to the PROBE TEST receptacle on the 5004A front panel. Push the probe tip point gently and firmly into the PROBE TEST receptacle until the point is help securely.
3. Connect the 5004A power cable to the correct power source and set the 5004A front panel as follows:

Test A

Switch Settings:

START:	IN
STOP:	IN
CLOCK:	IN or OUT

Displays:

Four seven-segment:	UP73 then ACA2
Gate:	flickers
Unstable Signature:	flickers except when good signature is on
Probe tip light:	Flickers when "ACA2" is on

Test B

Switch Settings:

START:	OUT
STOP:	OUT
CLOCK:	IN or OUT

Displays:

Four seven-segment:	3951 then 2P61
Gate:	flickers
Unstable Signature:	flickers except when good signature is on
Probe tip light:	Flickers when "2P61" is on

Note

In SELF-TEST mode, the seven-segment displays first have all seven segments lit dimly for about 1 second (tests all segments) and then have one of the signature sets listed above for about 1 second. If the probe RESET switch is pressed during the SELF-TEST mode, the four 7-segment-digit displays will show all zeros except when all segments are dimly lit.

Connecting the HP5004A Signature Analyzer to the Exorcisor

1. Connect the 5004A's grabber connectors as follows:

    CLK (yellow) clip to Exorcisor CLK terminal,
    START (green) clip to Exorcisor START/STOP terminal,
    STOP (red) clip to Exorcisor START/STOP terminal,
    GND (black) clip to Exorcisor GND terminal.

2. Connect The Exorcisor's +5V banana jack to the 5 volt source, either from the Cinematronics power supply or a lab supply. In the same manner connect the GND banana jack to the supply's GROUND connection. Verify that the board under test is connected to the +5 volt supply also.

3. Using a short jumper lead connect the Exorcisor's CLK terminal to the CLK test point on the logic board. This point is located between IC's Jx and Kx and is marked CLK on the component side of the board.

At this point the Exorcisor has all the necessary inputs connected to perform an operational verification test. If this test is not necessary skip the next section.

Verifying the Exorcisor output signatures

With the equipment connected as described in the previous section apply power to the +5V power supply. Verify that the supply is still putting out +5.0 volts DC ± 0.25VDC. Set the switches on the signature analyzer as follows:

HP5004A Switch Settings:

START:	IN (negative edge)
STOP:	OUT (positive edge)
CLOCK:	OUT (positive edge)

With the analyzer's data probe verify the following signatures at the specified locations:

DIP plug D8	pin	signature
	#4	7825
	#5	655C
	#9	802H
	#10	6PF3
	#11	8UC2
	#14	2518
	#15	0000
	#16	U6HH

Verifying the Exorcisor output signatures (cnt'd)

DIP plug U14	pin	signature
	#9	5555
	#10	CCCC
	#11	7F7F
	#12	5H21
	#13	0AFA
	#14	UPFH
	#15	52F8
	#16	HC89

DIP clip N2	pin	signature
	#4	F469
	#7	PH6F
	#9	211U
	#12	H28U

DIP clip R2	pin	signature
	#4	A69C
	#7	47F6
	#9	8CC5
	#12	510F

Dip clip T2	pin	signature
	#4	615F
	#7	A928
	#9	A29F
	#12	96FC

Preliminary CPU Operational Testing

There is a certain minimum operation level which the CPU board must meet before the Exorcisor can be used for fault diagnostics. The 20MHz oscillator circuit (IC-I2, XTAL, R2, R3 and C59) must be operating. The IC's H2 (74S113) and J4 (74265) must also be operational and generating the four clock signals CLK1, /CLK1, CLK2 and /CLK2. Refer to Sheet 1 of the schematics and, with the oscilloscope, verify that these clock signals are present. Note that the CLK1 signal's amplitude will be attenuated when the Exorcisor is connected, this is normal. The signal '**POWER_UP'** at IC B6 pin 2 (74LS04) must be at a TTL High ($V_o \geq 2V$). If these requirements are not met the Exorcisor will not operate. These circuits must be repaired before the Exorcisor can be used.

Connecting the Exorcisor to the Board Under Test

IMPORTANT!
Before you connect the Exorcisor verify that the 5 volt power supply is turned OFF!

Connecting the Exorcisor to the CPU is a simple task. First disconnect the ribbon cable which connects to the display. Then remove the two 16-pin DIP shunts located at D8 and U14. Connect the DIP plug at the end of the cable which plugs into J3 of the Exorcisor into the IC socket at D8. Connect the other DIP plug at the end of the cable which plugs into J1 into the socket at U14. Attach the DIP clip designated N2 to the IC-N2 (74LS257) paying close attention to the location of pin 1. Attach the R2 DIP clip to IC-R2 and the T2 DIP clip to IC-T2. There is a flying ball-clip connected to the cable from J1, this clip is attached to the test point TP8. No IC's need to be removed from the board in order to use the Exorcisor.

READING SIGNATURES AND VERIFICATION

With the equipment hooked up as described in the previous sections turn on the power to the analyzer and the DC power supply. Set the Signature Analyzer to the configuration shown below. Debugging is now a simple matter of touching the probe tip to a specific IC pin and comparing it's signature to that shown on the schematic. The expected signatures are listed in Appendix A for reference. The key below defines the terms used in the tables.

HP5004A Switch Settings:

START:	IN (negative edge)
STOP:	OUT (positive edge)
CLOCK:	OUT (positive edge)

NOTE: Some circuit nodes have two signatures shown, the upper (first) value is read when the CLOCK is positive edge triggered and the lower (second) value when the CLOCK is negative edge triggered.

Detecting faulty devices

In most cases detecting a defective device is as simple as finding a bad signature and finding the IC which is driving the node. Once you find a bad signature follow the signal 'up-stream' to the first IC at which a bad signature shows up at. If all the input signatures to this IC are correct and the output is not there a good chance you've found a bad device. This reasoning may not lead to a correct determination if, for instance, there is a short affecting the bad node or if an IC connected to the node has a shorted input. It's

always a good idea to check the node in question with a meter and an oscilloscope to help further diagnose a problem.

Testing the board for Non-JMI mode

Some of the signatures listed in Appendix A are shown within two forward slashes (/nnnn/). These are signatures read when the board has been put in the non-JMI mode. The JMI jumper must be removed, if present, to obtain these signatures. Be sure to replace this jumper when testing has been completed.

Testing the board's RAM Addressing Signatures

There are eight unique signatures in Appendix A shown with an asterisk (∗) prefix. These are the signatures for the eight RAM address lines, A0 thru A7. To obtain these signatures pin 10 of IC I12 and pin 10 of IC J12 must be tied to ground. These pins are connected together by a trace so it's only necessary to ground one. This can be done simply by using a 16-pin DIP clip with pins 10 and 8 tied together and placing the clip on either IC I12 or J12.

Tips & Techniques

The IC's on the Cinematronics CPU board have reference designations that correspond to their X and Y position on the board. The grid lines are designated U thru A across the wide dimension (horizontal if the board is positioned with the connectors along the top) and 2 thru 14 across the shorter (vertical) width. Unfortunately, there are no reference designations shown on the board for each IC. To speed up the debug process I ***highly*** recommend placing a small label on various IC's and marking them with it's reference designation and the number of pins the IC has. The small (5/8" x 3/16") IC labels that are available in 8 ½" X 11" sheets with 480 labels each are ideal.

Always check the test point marked C3-2P first. This is the RESET node and it's signature should be 'C32P'. If the signature is incorrect repair the reset circuit before continuing.

Always trace bad signatures in the opposite direction of the signal flow. A good starting point is at the X and Y data output latches and the line intensity control circuit.

A bad signature at an input of an IC will not *always* cause a bad signature at it's output.

An inverted signal will always have the same signature as it's non-inverted source signal.

Appendix A

Schematic: SHT1

IC #	PIN #	IC TYPE	SIGNATURE
B4	13	74LS00	A328
B4	11		A328
B4	1		Lo
B4	6		Hi
E4	7	74LS151	49P2
E4	11		PH07
E4	10		29A9
E4	9		80HP
E4	5		49P2
F4	9	74LS10	49P2
F4	10		392C
F4	11		392C
F4	8		A522
D4	5	74LS151	A522
B6	11	74LS04	392C
B6	10		392C
C4	5	74LS151	392C
F6	9	74LS27	49P2
F6	10		A522
F6	11		392C
F6	8		Lo
A6	8	74LS02	Lo
A6	9		9069
A6	10		9069
B6	13	74LS04	H28U
B6	12		H28U
F2	1	74LS259	PH07
F2	2		29A9
F2	3		80HP
F2	13		H28U
F2	14		0000
F2	4		FH1H
F2	5		54P5
F2	6		8CAU
F2	7		2043
F2	9		A941
F2	10		A328
F2	11		C9UC
F2	12		82CU

Schematic: SHT2

IC #	PIN #	IC TYPE	SIGNATURE
T2	1	74LS257	49P2
T2	2		HAFA
T2	5		UAC5
T2	11		651H
T2	14		F567
T2	3		F6A4
T2	6		HA32
T2	10		F97P
T2	13		0C22
T2	15		Hi
T2	4		615F
T2	7		A928
T2	9		A29F
T2	12		96FC
R2	1	74LS257	49P2
R2	2		9172
R2	5		711H
R2	11		FPF2
R2	14		HAC9
R2	3		P38A
R2	6		30CC
R2	10		FUC5
R2	13		725C
R2	15		Hi
R2	4		A69C
R2	7		47F6
R2	9		8CC5
R2	12		510F
N2	1	74LS257	49P2
N2	2		26PP
N2	5		67HU
N2	11		166U
N2	14		C432
N2	3		OU1F
N2	6		0841
N2	10		242C
N2	13		AC5H
N2	15		Hi
N2	4		F469

Appendix A (cnt'd)

Schematic: SHT2

IC #	PIN #	IC TYPE	SIGNATURE
N2	7	74LS257	PH6F
N2	9		211U
N2	12		H28U
K2	12	74LS32	7P23
K2	13		49P2
K2	11		7P23
L2	9	74LS10	clk1
L2	10		F1CH
L2	11		7P23
T4	3	74LS194	1C14
T4	4		8236
T4	5		304P
T4	6		FC6A
T4	10		2H8F
T4	9		C5F6
T4	7		HAFA
T4	2		9172
T4	12		HAFA
T4	13		UAC5
T4	14		651H
T4	15		F567
R4	3	74LS194	F43F
R4	4		5000
R4	5		34CP
R4	6		66UU
R4	10		2H8F
R4	9		C5F6
R4	7		F567
R4	2		26PP
R4	12		9172
R4	13		711H
R4	14		FPF2
R4	15		HAC9
N4	3	74LS194	9115
N4	4		61CA
N4	5		91CC
N4	6		6121
N4	10		2H8F

IC #	PIN #	IC TYPE	SIGNATURE
N4	9	74LS194	C5F6
N4	7		HAC9
N4	2		Lo
N4	12		26PP
N4	13		67HU
N4	14		166U
N4	15		C432
J6	1	74LS00	7P23
J6	2		C432
J6	3		0A76
J6	4		F6A4
J6	5		41UC
J6	6		FC5H
J6	9		FC5H
J6	10		0A76
J6	8		F12C
L2	3	74LS10	49P2
L2	4		F1CH
L2	5		clk2
S4	3	74LS194	1C14
S4	4		8236
S4	5		304P
S4	6		FC6A
S4	10		2H8F
S4	9		C5F6
S4	7		F12C
S4	2		P38A
S4	12		F6A4
S4	13		HA32
S4	14		F97P
S4	15		0C22
P4	3	74LS194	F43F
P4	4		5000
P4	5		34CP
P4	6		66UU
P4	10		2H8F
P4	9		C5F6
P4	7		0C22

Appendix A (cnt'd)

Schematic: SHT2 & SHT3

IC #	PIN #	IC TYPE	SIGNATURE
P4	2	74LS194	0U1F
P4	12		P38A
P4	13		30CC
P4	14		FUC5
P4	15		725C
M4	3	74LS194	9115
M4	4		61CA
M4	5		91CC
M4	6		6121
M4	10		2H8F
M4	9		C5F6
M4	7		725C
M4	12		0U1F
M4	13		0841
M4	14		242C
M4	15		AC5H
H12	3	74LS194	392C
H12	4		80HP
H12	5		29A9
H12	6		PH07
H12	9&10		CH9A
H12	12		0PH1
H12	13		54CC
H12	14		H255
H12	15		7H33
J12	3	74LS298	7H33
J12	4		H255
J12	5		54CC
J12	7		0PH1
J12	10		AAP8
J12	11		0000
J12	12		∗PF3C
J12	13		∗UCCC
J12	14		∗6034
J12	15		∗0038
I12	3	74LS298	392C
I12	4		80HP
I12	5		29A9

SHT3

IC #	PIN #	IC TYPE	SIGNATURE
I12	7	74LS298	PH07
I12	10		AAP8
I12	11		0000
I12	12		∗F6C6
I12	13		∗402U
I12	14		∗01F4
I12	15		∗PPC3
E12	1	74LS04	4A50
E12	2&3		4A50
E12	4		4A50
N14	20	9101C	4A50
N14	9		96FC
N14	11		A29F
N14	13		A928
N14	15		615F
N14	1		∗0038
N14	2		∗6034
N14	3		∗UCCC
N14	4		∗PF3C
N14	5		∗PPC3
N14	6		∗01F4
N14	7		∗402U
N14	21		∗F6C6
M14	20	9101C	4A50
M14	9		510F
M14	11		8CC5
M14	13		47F6
M14	15		A69C
M14	1		∗0038
M14	2		∗6034
M14	3		∗UCCC
M14	4		∗PF3C
M14	5		∗PPC3
M14	6		∗01F4
M14	7		∗402U
M14	21		∗F6C6
L14	20	9101C	4A50
L14	9		H28U
L14	11		211U

Appendix A (cnt'd)

Schematic: SHT3

IC #	PIN #	IC TYPE	SIGNATURE
L14	13	9101C	PH6F
L14	15		F469
L14	1		∗0038
L14	2		∗6034
L14	3		∗UCCC
L14	4		∗PF3C
L14	5		∗PPC3
L14	6		∗01F4
L14	7		∗402U
L14	21		∗F6C6
N11	3	74LS157	392C
N11	6		80HP
N11	10		29A9
N11	13		PH07
N11	15		4UHF
N11	4		8C81
N11	7		C428
N11	9		9AC5
N11	12		67C8
M11	3	74LS157	37C1
M11	6		HP4P
M11	10		P75P
M11	13		A6HF
M11	15		3P10
M11	4		C781
M11	7		6C47
M11	9		A8H3
M11	12		0PF5
L11	3	74LS157	392C
L11	6		80HP
L11	10		29A9
L11	13		PH07
L11	15		7323
L11	4		P9UF
L11	7		A996
L11	9		6HF3
L11	12		76F5
H10	4	74LS32	9069
H10	5		76F5

IC #	PIN #	IC TYPE	SIGNATURE
H10	6	74LS32	P6AF
N9	1	74LS85	8C81
N9	2		9398
N9	3		9686
N9	4		051P
N9	9		1776
N9	10		H9P9
N9	11		9AC5
N9	12		A29F
N9	13		A928
N9	14		C428
N9	15		615F
N9	5		A197
N9	6		237P
M9	1	74LS85	67C8
M9	2		0PF5
M9	3		Lo
M9	4		510F
M9	9		A8H3
M9	10		8CC5
M9	11		6C47
M9	12		47F6
M9	13		A69C
M9	14		C781
M9	15		96FC
M9	5		H9P9
L9	1	74LS85	P9UF
L9	9		96AF
L9	10		H28U
L9	11		6HF3
L9	12		211U
L9	13		PH6F
L9	14		A996
L9	15		F469
L9	5		051P
L9	6		9686
N6	1	25LS181	67C8
N6	2		96FC
N6	3		60P1

Appendix A (cnt'd)

Schematic: SHT3

IC #	PIN #	IC TYPE	SIGNATURE
N6	4	25LS181	60P1
N6	5		211A
N6	6		HC91
N6	7		H3UF
N6	8		41UC
N6	18		8C81
N6	19		615F
N6	20		C428
N6	21		A928
N6	22		9AC5
N6	23		A29F
N6	9		1C14
N6	10		8236
N6	11		304P
N6	13		FC6A
N6	15		7A6F
N6	17		3H1C
M6	1	25LS181	0PF5
M6	2		510F
M6	3		60P1
M6	4		60P1
M6	5		211A
M6	6		HC91
M6	7		2632
M6	8		41UC
M6	18		C781
M6	19		A69C
M6	20		6C47
M6	21		47F6
M6	22		A8H3
M6	23		8CC5
M6	9		F43F
M6	10		5000
M6	11		34CP
M6	13		66UU
M6	15		6023
M6	17		70AF
L6	1	25LS181	P6AF
L6	2		H28U

IC #	PIN #	IC TYPE	SIGNATURE
L6	3	25LS181	60P1
L6	4		60P1
L6	5		211A
L6	6		HC91
L6	7		9A6A
L6	8		41UC
L6	18		P9UF
L6	19		F469
L6	20		A996
L6	21		PH6F
L6	22		6HF3
L6	23		211U
L6	9		9115
L6	10		61CA
L6	11		91CC
L6	13		6121
L6	15		235P
L6	17		21H0
U2	9	74S04	9A6A
U2	8		9A6A
K2	4	74LS32	41UC
K2	5		9A6A
K2	6		60P1
K2	9		9A6A
K2	10		41UC
K2	8		211A
K4	2	74LS02	41UC
K4	3		9A6A
K4	1		60P1
J8	1	74LS86	41UC
J8	2		9A6A
J8	3		HC91
U9	4 & 13	74LS75	0000/H33C
U9	4 & 13		[5A4H]
T9	4 & 13	74LS75	0000/H33C
T9	4 & 13		[5A4H]

Appendix A (cnt'd)

SHT4

IC #	PIN #	IC TYPE	SIGNATURE
U11	1	74LS157	90AP
U11	15		C32P
T11	1	74LS157	90AP
T11	15		C32P
T13	1	74LS377	802H
T13	3		HC89
T13	4		UPFH
T13	7		5H21
T13	8		CCCC
T13	13		5555
T13	14		7F7F
T13	17		0AFA
T13	18		52F8
T13	2		6H37
T13	5		1F1A
T13	6		4C4H
T13	9		4819
T13	12		5547
T13	15		1106
T13	16		8884
T13	19		C004
S13	1	74LS377	6PF3
S13	2		PH07
S13	5		29A9
S13	6		80HP
S13	9		392C
S13	12		A6HF
S13	15		P75P
S13	16		HP4P
S13	19		37C1
J14	10	74S288	655C
J14	11		7825
J14	12		6PF3
J14	13		390P
J14	14		19AP
J14	1		H666
J14	2		FU3U

IC #	PIN #	IC TYPE	SIGNATURE
J14	3	74S288	P503
J14	4		C15P
J14	5		90AP
H14	2	74S02	P503
H14	3		U646
H14	1		FU1U
I14	1	74LS163	C32P
I14	3		H666
I14	6		FU3U
I14	9		FU1U
I14	7 & 10		891F
I14	11		6069
I14	12		891F
I8	9	74LS04	891F
I8	8		891F
I10	13	74S00	19AP
I10	12		6069
I10	11		6909
H14	11	74S02	5278
H14	12		6909
H14	13		H33C
H14	9		H33C
H14	8		891F
H14	10		07U2
H14	5		H33C
H14	4		0000 / H33C
I8	3	74LS04	2518
I8	4		2518
J4	1	74265	578F
J4	2		578F
J10	1	74LS107	54CC
J10	4		0PH1
J10	12		FFC9
J10	13		C32P
J10	3		473U
J10	2		473U

Appendix A (cnt'd)

Schematic: SHT4

IC #	PIN #	IC TYPE	SIGNATURE
P13	3	74LS194	P6AF
P13	4		6HF3

IC #	PIN #	IC TYPE	SIGNATURE
R11	5		UHUH
R11	6		U095

P13	5		A996
P13	6		P9UF
P13	9 & 10		FP22
P13	12		480P
P13	13		70F4
P13	14		98A7
P13	15		H9FP
R13	3	74LS377	0PF5
R13	4		A8H3
R13	7		6C47
R13	8		C781
R13	13		67C8
R13	14		9AC5
R13	17		C428
R13	18		8C81
R13	2		9UCC
R13	5		P6A0
R13	6		UHUH
R13	9		U095
R13	12		2788
R13	15		1533
R13	16		42P0
R13	19		9U76
S11	3	74LS163	H9FP
S11	4		98A7
S11	5		70F4
S11	6		480P
S11	1		C32P
S11	2		clk1
S11	9		390P
S11	7		C15P
S11	11		99F8
S11	12		2CAP
S11	13		38P3
S11	14		5278
R11	3	74LS163	9UCC
R11	4		P6A0

R11	11		9HPH
R11	12		50HC
R11	13		F0A5
R11	14		45H9
P11	3	74LS163	2788
P11	4		1533
P11	5		42P0
P11	6		9U76
P11	11		63P6
P11	12		CC8C
P11	13		C8PU
P11	14		6865
S9	1	74LS157	19AP
S9	2		H28U
S9	5		211U
S9	11		PH6F
S9	14		F469
S9	4		155C
S9	7		7211
S9	9		8066
S9	12		HA00
R9	2	74LS157	510F
R9	5		8CC5
R9	11		47F6
R9	14		A69C
R9	4		UPAP
R9	7		A7U5
R9	9		5PF5
R9	12		FC92
P9	2	74LS157	96FC
P9	5		A2F9
P9	11		A928
P9	14		615F
P9	4		C443
P9	7		U62F
P9	9		0499
P9	12		578F

Appendix A (cnt'd)

Schematic: SHT5

IC #	PIN #	IC TYPE	SIGNATURE
G12	3	74S10	C004
G12	4		8884
G12	5		1106
G12	6		U24U
G14	2	74S158	6H37
G14	5		1F1A
G14	11		4C4H
G14	14		4819
G14	3		5547
G14	6		1106
G14	10		8884
G14	13		C004
G14	4		2293
G14	7		62C7
G14	9		P68U
G14	12		283P
F14	1	74S287	9673
F14	2		51C4
F14	3		U24U
F14	4		283P
F14	5		2293
F14	6		62C7
F14	7		P68U
F14	15		2518
F14	9		1846
F14	10		FP05
F14	11		8399
F14	12		61C3
E14	10	74S288	2293
E14	11		62C7
E14	12		P68U
E14	13		283P
E14	14		U24U
E14	1		0C45
E14	2		320U
E14	3		C530
E14	4		1P02
E14	5		394A
E14	6		8PP6

IC #	PIN #	IC TYPE	SIGNATURE
E14	7	74S288	409C
E14	9		07PU
D14	1	74S288	2H8F
D14	2		A76P
D14	3		41UC
D14	4		7P23
D14	5		9A6A
D14	6		5H61
D14	7		8ACC
D14	9		5AA5
C14	1	74S288	9069
C14	2		7323
C14	3		CH9A
C14	4		96UA
C14	5		67AH
C14	6		2PFF
C14	7		32U4
C14	9		U100
E10	9	74LS163	802H
E10	7		8UC2
E10	13		9673
E10	14		51C4
D10	1	74LS04	7341
B6	9		615F
B6	8		615F [0000]
A8	8	74LS107	615F [0000]
A8	11		615F [0000]
A8	5		30AP [Hi]
G10	3	74LS194	A197
G10	4		2379
G10	5		AH4H
G10	6		AC5H
G10	9 & 10		F1CH
G10	12		0F96
G10	13		4U54
G10	14		8233
G10	15		8H73

Appendix A (cnt'd)

Schematic: SHT5

IC #	PIN #	IC TYPE	SIGNATURE
U7,R7	1	ROM	C443
T7,P7	2		FC92
"	3		5PF5
"	4		A7U5
"	5		UPAP
"	6		HA00
"	7		8066
"	8		7211
"	18		473U
"	19		578F
"	20		Lo
"	21		Lo
"	22		0499
"	23		U62F
A8	8	74LS107	/ 0000 /
A8	11		/ 0000 /
A8	5		/ Hi /
F10	6	74LS151	/ 61H3 /
A12	3	74LS32	/ 2AF1 /
S11	9	74LS163	/ 2AF1 /
S11	15		/ 2F0H /
S11	11		/ 73HU /
S11	12		/ F745 /
S11	13		
S11	14		
R11	9		/ 2AF1 /
R11	15		/ HA98 /
R11	11		/ P781 /
R11	12		/ 8HA7 /
R11	13		/ AC18 /
R11	14		/ F55H /
P11	9		/ 2AF1 /
P11	11		/ 7C77 /
P11	12		/ 17UP /
P11	13		/ C962 /
P11	14		/ 9855 /
S9	4	74LS157	/ 9515 /
S9	7		/ U801 /

IC #	PIN #	IC TYPE	SIGNATURE
S9	9	74LS157	/ 1285 /
S9	12		/ UUF5 /
R9	4	74LS157	/ 0A1F /
R9	7		/ H162 /
R9	9		/ FF86 /
R9	12		/ FA45 /
P9	4	74LS157	/ 4473 /
P9	7		/ 3124 /
P9	9		/ A8PF /
P9	12		/ 4U1H /
U9,T9	4,13	74LS75	/ 5AH4 /
J14	13	74S288	/ 2AF1 /
J14	1		/ 86F5 /
J14	2		/ UUPU /
J14	3		/ A9P3 /
H14	1	74S02	/ 83UU /
H14	5		/ 5AH4 /
H14	4		/ 5AH4 /
H14	11		/ A98H /
H14	12		/ 8P9C /
H14	13		/ 5AH4 /
H14	10		/ HOU8 /
I14	7,10	74LS163	/ 6HH2 /
I14	11		/ 87UC /
I14	12		/ 6HH2 /
U7,R7	1	PROMS	/ 4473 /
T7,P7	2		/ FA45 /
"	3		/ FF86 /
"	4		/ H162 /
"	5		/ 0A1F /
"	6		/ UUF5 /
"	7		/ 1285 /
"	8		/ U801 /
"	19		/ 4U1H /
"	22		/ A8PF /
"	23		/ 3124 /

Appendix A (cnt'd)

Schematic: SHT5

IC #	PIN #	IC TYPE	SIGNATURE
F10	3	74LS151	30AP [Hi]
F10	2		018F
F10	1		8H73
F10	9		4C4H
F10	10		1F1A
F10	11		6H37
F10	13		0F96
F10	14		4U54
F10	15		8233
F10	6		F384 [61H3]
A12	2	74LS32	67AH
A12	3		390P [2AF1]
C10	9	74LS08	2PFF
C10	10		7341
C10	8		U646
B8	10	74LS107	C32P
B8	11		6PF3
B8	5		19AP
B8	6		19AP
B8	1		409C
B8	4		802H
B8	2		4A50
E12	5	74LS04	5547
E12	6		5547
A10	9	74LS00	2518
A10	10		51C4
A10	8		36C4
D12	3	74LS27	4819
D12	4		67AH
D12	5		36C4
D12	6		Lo
D12	9		5547
D12	10		36C4
D12	11		8PP6
D12	8		Lo
B10	13	74LS32	32U4
B10	11		32U4

IC #	PIN #	IC TYPE	SIGNATURE
C10	11	74LS08	Lo
D10	12	74LS02	C32P
D10	13		C32P
A8	1		32U4
A8	4		802H
A8	2		49P2
A8	3		49P2
C8	12	74LS107	U6HH
C8	13		C32P
C8	3		9081
C8	11		665F
C8	8		C32P
C8	10		Hi
C8	6		C32P
C8	5		C32P
F12	1	7425	6H37
F12	2		4819
F12	4		1F1A
F12	5		FC4H
F12	6		8884
I10	3	74LS00	0000 / PC9U
D10	5	74LS02	67AH
D10	4		FFC9
F12	10	7425	8884
F12	12		C004
F12	13		2518
F12	8		774P
D10	8		774P
D10	9		6598
D10	10		~12H6~
A14	1	74S08	51C4
A14	2		32U4
A14	3		12A8
B12	9	74LS10	2518
B12	11		0F96
B12	8		C05P
A12	6	74LS32	A76P

Appendix A (cnt'd)

Schematic: SHT5

IC #	PIN #	IC TYPE	SIGNATURE
K4	8	74LS02	CUH7
K4	9		0UHA
K4	10		AA31
C12	1	74LS27	1P02
C12	2		2518
C12	12		C4AF
C12	3		2518
C12	4		U6HH
C12	5		96UA
C12	6		H47A
C12	10		774P
C12	8		1798
B12	3	74LS10	C32P
B12	4		FP05
B12	5		1798
B12	6		077H
A10	12	74LS00	802H
A10	11		802H
A10	4		1798
A10	5		1846
A10	6		7890
A10	1		6PF3
A10	3		6PF3
A6	5	74LS02	1846
A6	6		U100
A6	4		AAP8
A14	4	74S08	320U
A14	5		7341
A14	6		F567
A12	10	74LS32	0C45
A12	8		FP22
B14	9	74S32	F567
B14	8		4UHF
B14	1		774P
B14	2		7323
B14	3		UC77
B14	5		F567
B14	6		3P10

SHT6

IC #	PIN #	IC TYPE	SIGNATURE
H8	5	74LS02	C530
H8	6		5547
H8	4		403F
I8	12	74LS04	403F
G8	4	74LS107	6598
G8	2		239A
F8	9	74LS163	C530
F8	7		F9U6
F8	1		C32P
F8	15		F9U6
B6	4	74LS04	F9U6
H8	11	74LS02	F9U6
H8	12		239A
H8	13		U97A
H8	8		5547
H8	9		C530
H8	10		U50F
G8	11	74LS107	0109
G8	5		018F
G8	6		018F
A12	12	74LS32	018F
A12	13		F9U6
A12	11		204A
I8	2	74LS04	204A
H8	1	74LS02	3980
J8	9	74LS86	F97P
J8	10		F6A4
J8	8		0UHA
J8	12		651H
J8	13		HAFA
J8	11		CUH7
F6	3	74LS27	1P02
F6	6		6598
I8	10	74LS04	6598
H6	13	74LS164	9820
J6	11	74LS10	9820
J2	3	74LS32	9820
J2	12	74LS32	C9UC
J2	11		2873

Appendix A (cnt'd)

Schematic: SHT6

IC #	PIN #	IC TYPE	SIGNATURE
E8	10	74S288	A8F6
E8	11		90P2
E8	12		7U69
E8	13		A19U
E8	14		0495
E8	1		5C13
E8	2		26U2
E8	3		1825
E8	4		9890
E8	5		AUH7
E8	6		673F
E8	7		FH67
E6	1	74LS163	403F
E6	7		3980
E6	9		6598
E6	11		90P2
E6	12		9620
E6	13		9170
E6	14		A8F6
E6	15		049C
D6	6	74LS163	A3U1
D6	11		PF0A
D6	12		A19U
D6	13		7U69
D6	14		FA81
D6	15		CH8U
C6	3	74LS163	1P24
C6	4		0495
C6	11		H3PU
C6	12		0495
C6	13		1P24
C6	14		A3U1
C6	15		0109
U2	11	74S04	F6A4
U2	10		F6A4
U2	13		HAFA
U2	12		HAFA
S2	1	74LS377	C530

IC #	PIN #	IC TYPE	SIGNATURE
S2	4	74LS377	F6A4
S2	14		HA32
S2	13		F97P
S2	17		0C22
S2	3		HAFA
S2	7		UAC5
S2	8		651H
S2	18		F567
S2	5		6P3U
S2	15		6P3U
S2	12		8A2A
S2	16		6P3U
S2	2		3796
S2	6		3796
S2	9		U366
S2	19		1H2A
P2	1	74LS377	C530
P2	4		P38A
P2	14		30CC
P2	13		FUC5
P2	17		725C
P2	3		9172
P2	7		711H
P2	8		FPF2
P2	18		HAC9
P2	5		6P3U
P2	15		0000
P2	12		P415
P2	16		6P3U
P2	2		2ACF
P2	6		1H2A
P2	9		C7P5
P2	19		AA58
M2	1	74LS377	C530
M2	4		OU1F
M2	14		0841
M2	13		242C
M2	17		AC5H
M2	3		26PP

Appendix A (cnt'd)

Schematic: SHT6

IC #	PIN #	IC TYPE	SIGNATURE
M2	7	74LS377	67HU
M2	8		166U
M2	18		C432
M2	5		8A2A
M2	15		6P3U
M2	12		8A2A
M2	16		0000
M2	2		0000
M2	6		C7P5
M2	9		PP4F
M2	19		0000
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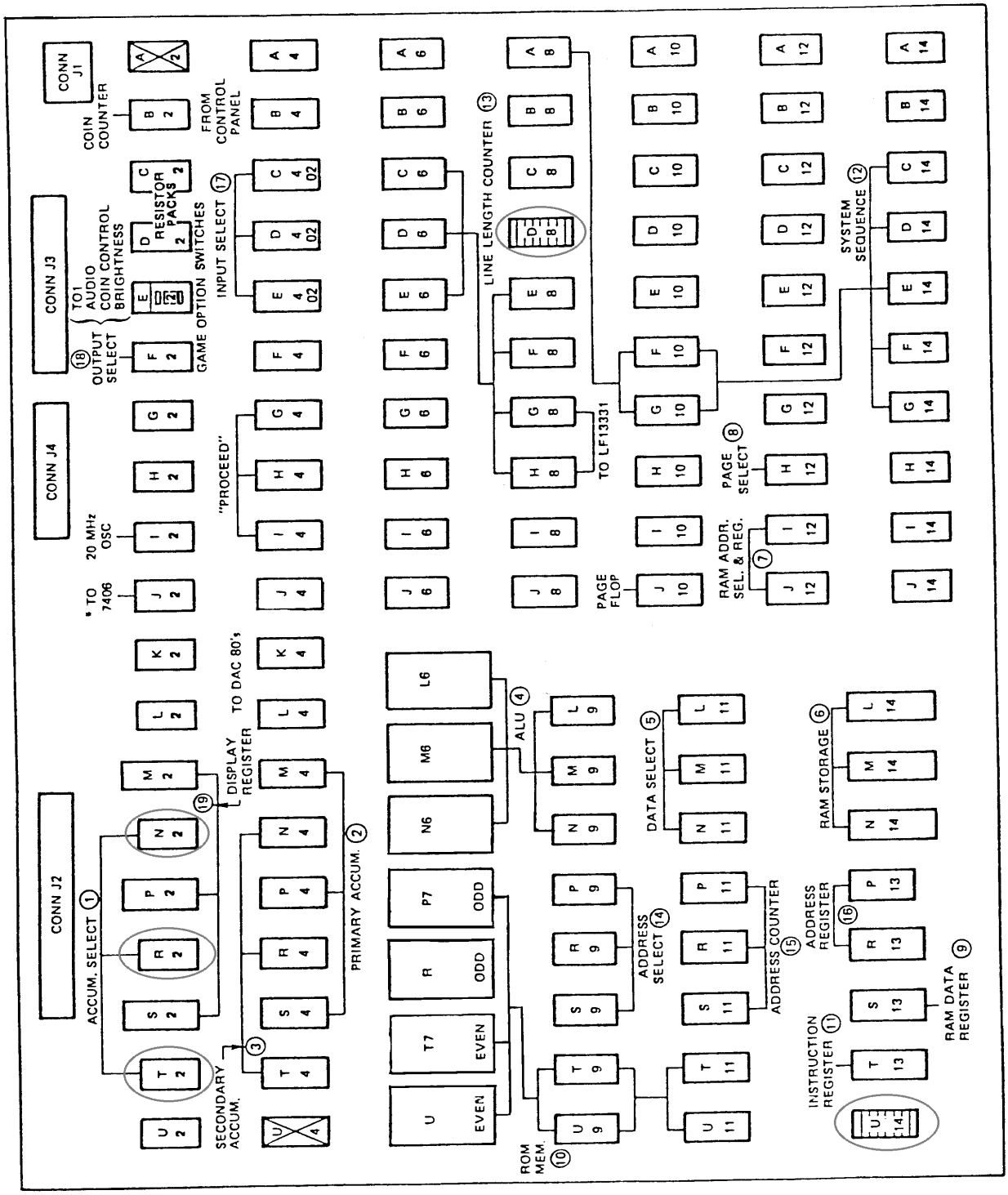
IC #	PIN #	IC TYPE	SIGNATURE

Key for Appendix A

clk1	CLOCK signal, will show ***0000*** signature
clk2	CLOCK signal, "
Hi	TTL level HIGH, "
Lo	TTL level LOW, "
nnnn / mmmm	Lower (2^{nd}) signature obtained with ⌐_ edge CLK (button IN)
∗nnnn	Signature obtained with J12 (& I12) pin 10 tied to GND
/nnnn/	Signature available with *NO JMI* option (jumper removed)

Appendix B


CONN J2
CONN J4
CONN J3
CONN J1
ACCUM. SELECT 1
SECONDARY ACCUM. 3
PRIMARY ACCUM. 2
DISPLAY REGISTER 19
TO DAC 80's
* TO 7406
20 MHz OSC
"PROCEED"
TO LF13331
LINE LENGTH COUNTER 13
PAGE FLOP
RAM ADDR. SEL. & REG. 7
PAGE SELECT 8
SYSTEM SEQUENCE 12
FROM CONTROL PANEL
COIN COUNTER
18 OUTPUT SELECT
TO1 AUDIO COIN CONTROL BRIGHTNESS
GAME OPTION SWITCHES
RESISTOR PACKS
INPUT SELECT 17
ALU 4
ROM MEM. 10
DATA SELECT 5
ADDRESS SELECT 14
ADDRESS COUNTER 15
ADDRESS REGISTER 16
RAM STORAGE 6
INSTRUCTION REGISTER 11
RAM DATA REGISTER 9
EVEN
ODD

Appendix C

EXAMPLES OF USEFUL MANUFACTURERS' LITERATURE

Schematic Package #72-10626-02 Rev J, *C.P.U. Schematic Diagram with Signatures*, Cinematronics Inc.

Application Note AN-222-4, *Guidelines for Signature Analysis: Understanding the Signature Measurement,* Hewlett-Packard Inc., Publication Number 5952-7684.

Application Note AN-222-6, *Troubleshooting with Composite Signatures,* Hewlett-Packard Inc., Publication Number 5952-7684.