performing 16 arithmetic operations determined by inputs S0, S1, S2 and S3. These inputs re decoded by devices K2. K4 and J8. The operations process either of the A and B ALU inputs. The carry outputs (lo) are tied to look-ahead carry device L4 to be discussed later. After the operation has been performed the outputs from these ALU devices (F0-F11) are then fed to the primary and secondary accumulaters provide two functions: a Y and an X shift register, and arithmetic accumulators. The primary accumulator is comprised of shift registers F4, P4 and M4 (74LS194's). These shift registers are tied together providing 12 bits of computational capability. This output addresses the ALU, the RAM and the ROM for look-up purposes. All of these outputs while in the display mode supply the X register with X data. The secondary accumulator operates very much like the primary and is

comprised of shift registers T4, R4 and N4. These also either address the program memory or provide data bits to the RAM and ALU depending on the state of the accumulator selector. The accumulator selector is comprised of data selector devices R2, N2 and T2 (74LS257). This data selector selects either input A or input B. Input A is the secondary accumulator bits SA0-SA11 and input B which the primary data bits PA0-PA11. These inputs are selectable by the select input line which originates from the A2 decoder (74LS107). When this bit is low it selects A input, when high it selects B input. Both select lines are commonly tied, therefore providing the identical select signal for N2, R2 or T2. The high speed look-ahead carry generator (74LS182) together with the ALU's provide a high speed ALU circuit.

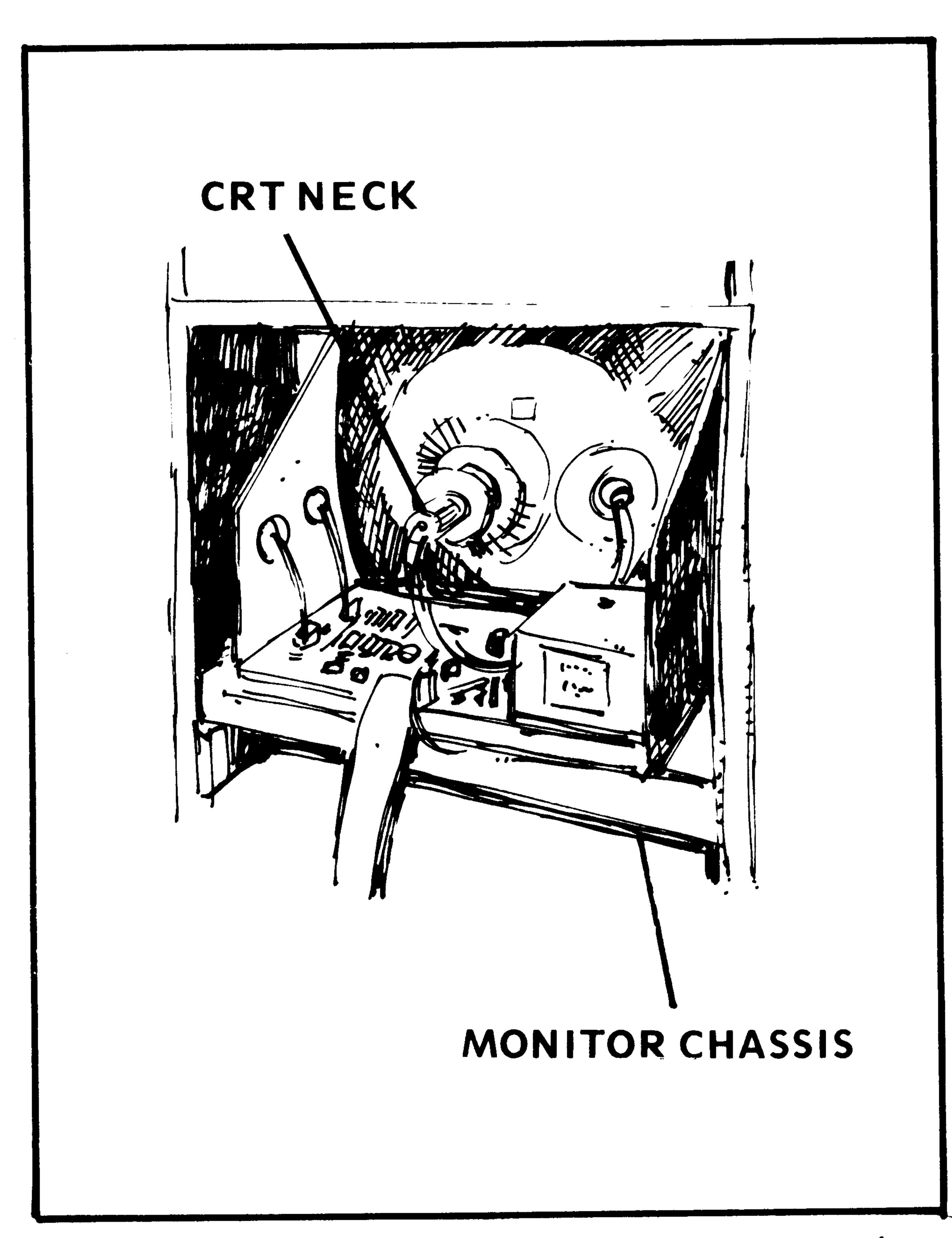


Figure 4-2 CRT Magnetic Centering Rings Location

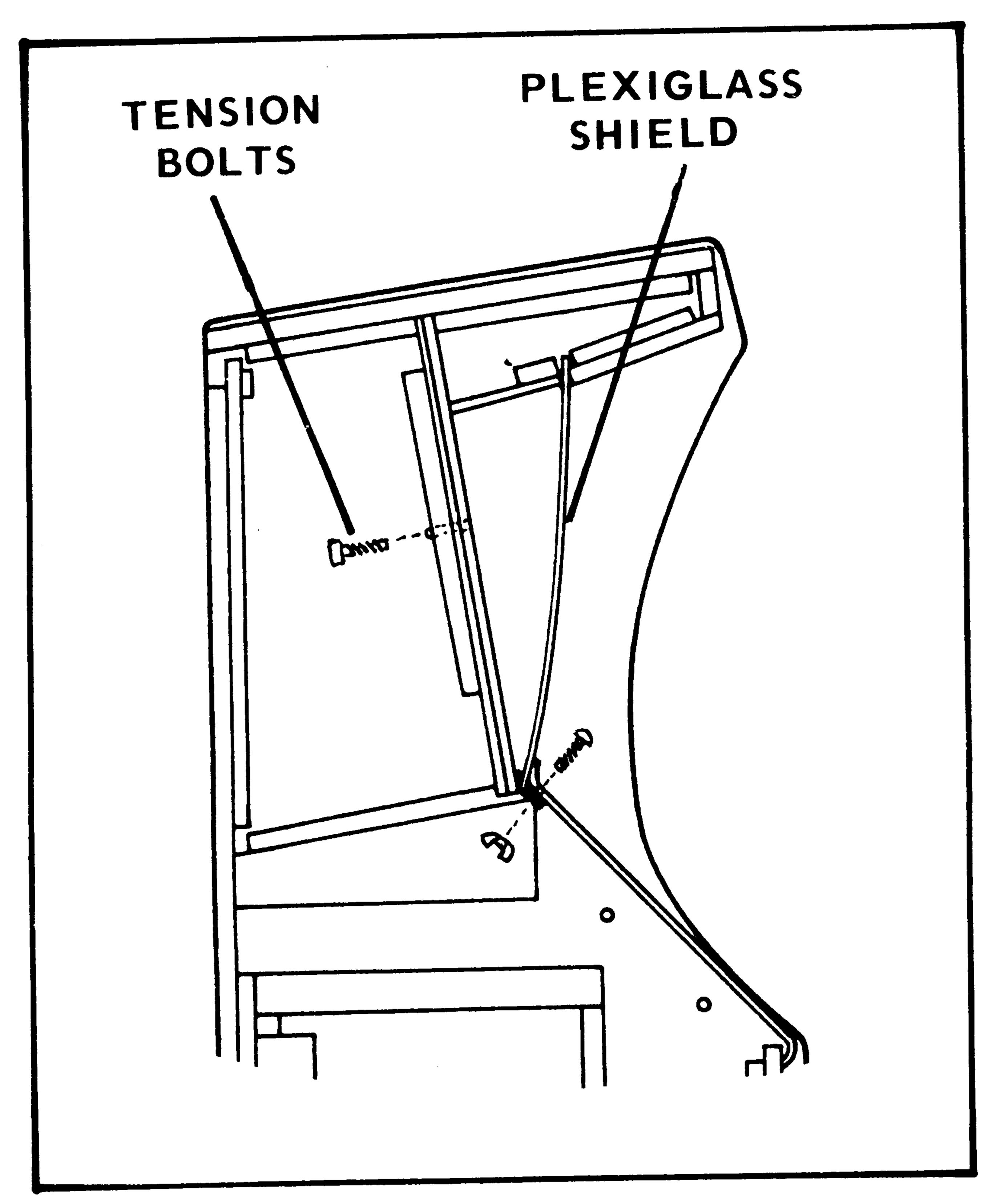


Figure 4-6 Plexiglass Shield and Plex Retainer Removal