The program memory is comprised of 2, 8 X 4K ROMS with two pages of memory in each: 1 even chip, 1 odd chip. The odd chip contains the odd memory and the even chip contains the even memory locations.

The Program Address Counter

(Refer to Appendix A, Figure A-5)

The program address counter is comprised of 4-bit binary counters S11, R11 and P11 (74LS163). These counters are presetable by the states of inputs at pin 3, 4, 5 and 6. The preset inputs originate from register devices P13 and R13 (74S377 and 74LS194 dual latch registers). These registers are loaded with the data from the output of the data selector (L0-L11) which originates from either the RAM or the ROM memory (see Figure A-6). When the register is loaded, the output presets the input to the program address counters. This preset input is loaded when pin 9 of each of the counter devices goes low. This preset input is the initial point from where the counters begin to count. The output of the program address counter, a sequential scheme, addresses the ROM program memory whenever the program address selector selects bus B. When A is selected it automatically is tied through the address bus to the ROM program memory. These counters carry output of each device (S11 the least signigicant device and P11 the most significant). The carry output of S11 triggers the R11 counter. Counter R11 reaches the count of 16 producing high carry output as a dignal t pin 10 to P11. This program address counter is capable of addressing all 4K words of memory in the ROM program memory.

Program Memory Data Bus Multiplexing

(Refer to Appendix A, Figure A-6)

The purpose of multiplexing the data bus from the program memory is to make 400NS chips look like 200NS chips. The data selector is comprised of devices T11 and U11 which are 2 to 1 data selector devices. When the A input to these two devices are selected it is the data currently processed at the output of the ROM program memory. When B is selected it is a delayed data structure. The outputs of these two data selector devices T11 and U11 form one data bus. The A or the B inputs to these data selectors are selected by the conditions of the outputs RESET, ODD and EVEN from devices U4. In this particular memory therefore the selection between inputs A and B means either the selection of the data from U7 (even) or from R7 (odd).

The Instruction Register

(Refer to Appendix A, Figure A-7)

The instruction register (T13) provides all of the instructions in nibbles (4-bits of an 8-bit word) to the system sequencer logic. These instructions are actual instructions required to systematically set up the game with all the actual event sequences for the board logic.

The Data Register

(Refer to Appendix A, Figure A-7)

The data address register (S13) provides the data from the program memory multiplexed to either the RAM memory or RAM address, the computation circuitry or the program address counter through the accumulator D0-D3 is used by the RAM working storage memory and all 8-bits are used by the computation circuitry. The instruction data line I1-I7 is multiplexed by device G14 (74LS158).

Working Storage, Address Selector and Register

(Refer to Appendix A, Figure A-8)

The working storage address selector and register circuitry, provide the RAM address A0-A7. These address bits locate a particular memory address to either "write" into or "read" out of the RAM. This circuit is comprised of register H12, and single 4-bit register and registers J12 and I12, dual selectable 4-bit registers. Register H12, the page register, matches data bits D0-D3 to the output of H12 (QA-QD). Data bits D0-D3 and the delayed data bits D0-D3 are the upper A, B, C and D inputs to devices J12 and I12. The lower A, B, C and D to J12 and I12 are the W0-W7 RAM outputs. These outputs are divided down into nibbles whereas the J12 A, B, C and D lower inputs are W4-W7 and the lower A, B, C and D inputs to R12 of W0-W3. These two quad 4-bit registers as selectable devices, therefore either the RAM output data or data register bits are selectable by the state of the select bit of pin 10, to address a given location in RAM memory.

The Data Selector

(Refer to Appendix A, Figure A-8)

The data selector circuitry is comprised of N11, M11 and L11 (74LS157). The purpose of this circuitry is to select either the data register data bits which are at the inputs of the computational circuitry devices or the RAM output data bits which are the A input to the data selector. The outputs of L11, M11 and N11 are the register preset inputs for the program address counter.

The Computation Circuitry

(Refer to Appendix A, Figure A-9)

The computation circuitry is the core of the entire logic PCB. The purpose of this circuitry is to appropriately process all the information in the data instruction to the logic PCB while controlled by the sequencer logic which provides all the timing and control signals to the game logic. The ALU, a major circuitcomponent is comprised of three ALU devices N6, M6 and L6. These ALU's have the capability of