Another spot kill protection circuit (Q21, Q23 and U6) keeps Q14 on when either intensity input is high but when both inputs are low it provides a 2 millisecond turn-on time for Q14. After the 2 millisecond period the Q21 device turns on removing the current path through Q20 and Q22 by turning off Q14. This is accomplished when pins 2 and 4 of U6 are both high which turns on Q23, inverts at pin 10 of U6. Pin 10 of U6 as it switches from a low to a high is initially at ground, then gradually goes positive at C18, until after approximately 2 milliseconds it is positive enough to turn on Q14.

(Refer to Appendix A, Figure A-2)

The schematic of Figure A-2 illustrates two identical circuits, one for the Y and the other for the X coordinate. For purposes of this explanation only the upper half will be discussed (the Y coordinant circuit of Figure 3.4). Beginning with the inputs we have 12, 6 inputs to DAC U5 defining the Y coordinate. These DAC's generate approximately 4096 (4K) different positions on the screen for the Y coordinate, likewise 4096 for the X coordinate at the lower half of the circuit. Supply voltage to these two DAC's (U6 and U1) originates from the +15 volt regulators of Figure A1 (U10 and U11). The analog output of DAC U5 enters the non-inverting input of amplifier U4 from either the analog Switch 1 or th analog Switch 2. Assume that 4 volts at the analog output (pin 15 of U5) and that analog Switch 2 has been enabled. The 4 volts applied to the input OP-AMP U4 also appears across capicitor C35. The output voltage at the circuit of U4 also appears at the wiper of potentiometer R54. The voltage at this wiper is applied to a discrete differential amplifier circuit comprised of device Q16, Q17 and Q18. The +4 volts turns on Q17 which also turns on transistor Q8. The input to this transistor is the output of the differential amplifier of Q17 and Q18. This output is then urrent boosted by the Q10 and Q110 devices for the positive transistion or by the Q6 and Q111 for the negative transitions. Devices Q9 and Q12 are the overload protection. The current then flows through the Y (vertical) deflection coil and back to the inverting input at the base of Q18 in the differential amplifier circuit which nulls out, providing a perfectly balanced current injection circuit. Nothing is displayed on the screen since there is no signal entering the normal or high intensity inputs of the modulator circuitry of Figure A-1. Switch 2 opens leaving the charged capacitor C35 with the initial voltage, which is the initial point of the line segment to be displayed on the CRT after Switch 2 is opened (Switch 1 also remains open). The terminal point of the line segment is entered into the Y register of the logic board and then loaded into the DAC. Assume 5 volts at the output of the DAC, Switch 1 is energized, making contact and appling the 5 volt output from the DAC to the non-inverting input of U4. This new

voltage is across the RC network comprised of R58, R59 and C35. The modulating circuits of sheet 1 of 2 turns on the electron beam current to the CRT providing a display from the initial point (voltage across C35) to the terminal point, voltage which has been loaded into the DAC from the Y register. The transition from the initial point to the terminal point appears as a straight line. The rate at which this line segment travels is determined by the RC network at the input of U4. When the register is changed to a new point, Switch 1 opens and Switch 2 closes which places the new value across C35. The initial voltage across C35 is never displayed on the CRT until a signal at the intensity modulator input turns on the electron beam current to the CRT. The lower half of this section for the X coordinate is identical.

THE VECTOR GENERATOR

The vector generator is the digital section of the vector display electronics located on the logic board. As illustrated in Figure 3.3, it shows the working storage register, program memory, arithmetic logic unit (ALU), the primary and secondary accumulators together with the accumulator selector and the system sequencer logic. The remaining logic circuitry which is the X and Y register and the line length timer are primarily used for the display functions and are not shared with the game logic.

Figure 3-4 extracts the digital display electronics from Figure 3-3 simplifying its explanation. The line length timer included in Figure 3-4 is divided into the decoderand counter of Figure 3-5. The purpose of the line length timer is to determine the duration of closure to the electron beam switch which allows a vector to be displayed on the CRT

The 12-bit presetable counter comprised of D6 and C6 is initially cleared (CLR) which sets it to zero. It then counts at the rate of the clock (CLK 8). The output of the counter addresses the preset decoder which produces outputs to the counter which are the preset inputs to the counter whenever a load signal goes low. This enable is removed when the line length counter reaches a maximum count.

THE GAME LOGIC Program Memory

A PROM PCB is temporarily used in place of the standard ROM devices (8, 8 X 1K EPROMS). This PCB is remote from the logic PCB mounted next to the audio PCB. When ROM's (permanent devices) are developed they are to be installed in their appropriate sockets and remove the PROM PCB.