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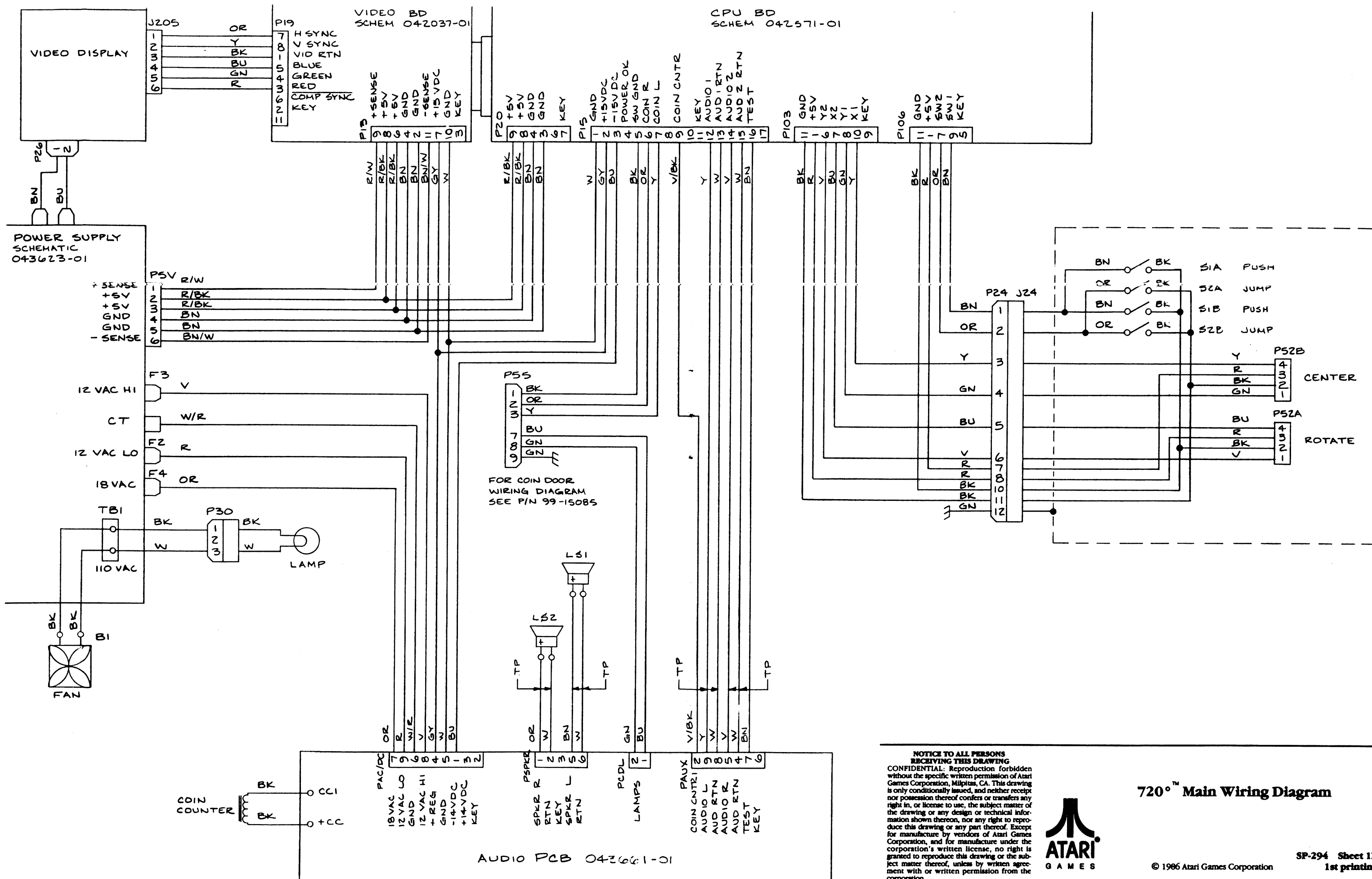
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Schematic Package Supplement to the 720°™ Operators Manual



NOTE
This staple temporarily holds the schematic package together. Remove the staple before using these schematics.

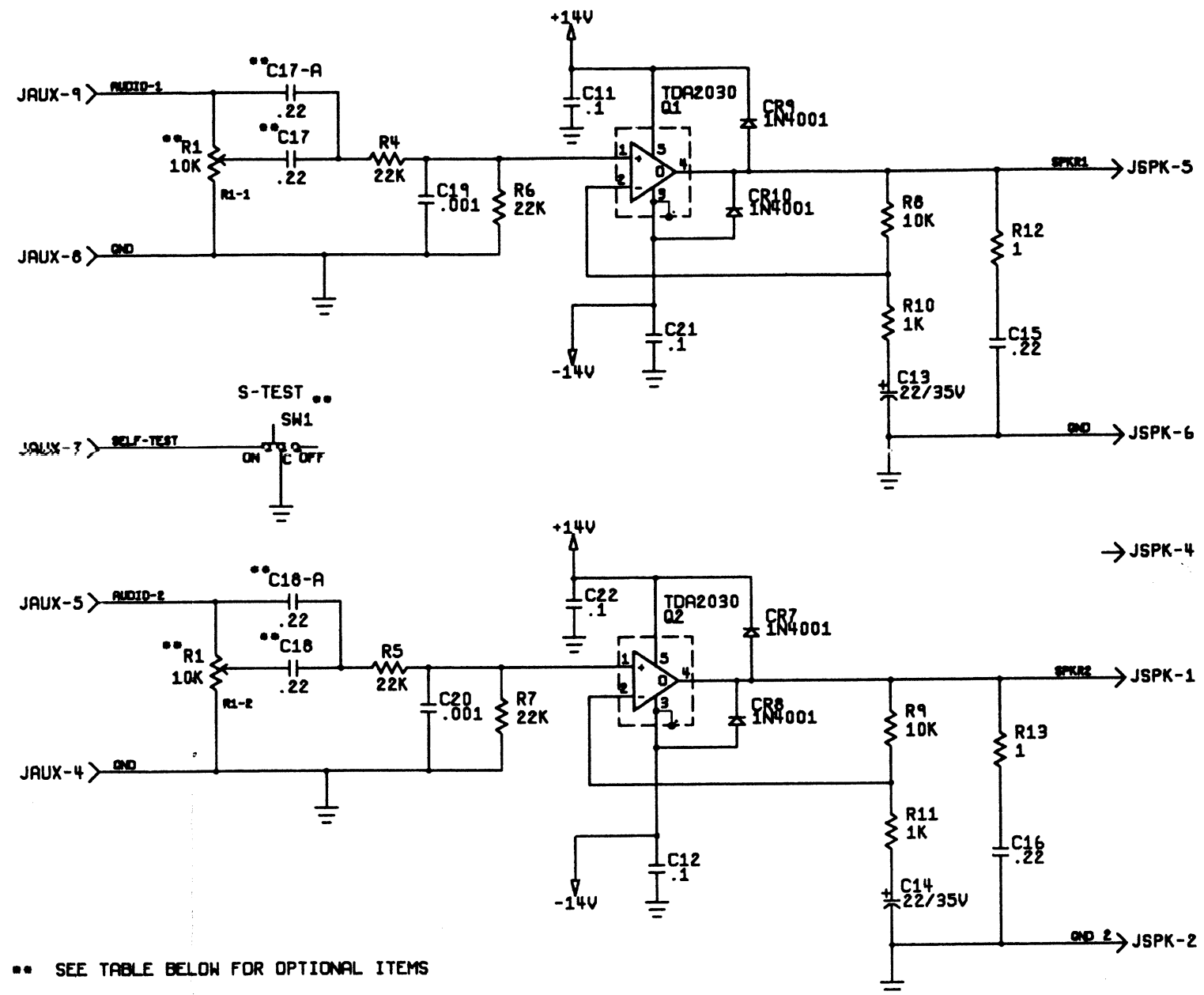
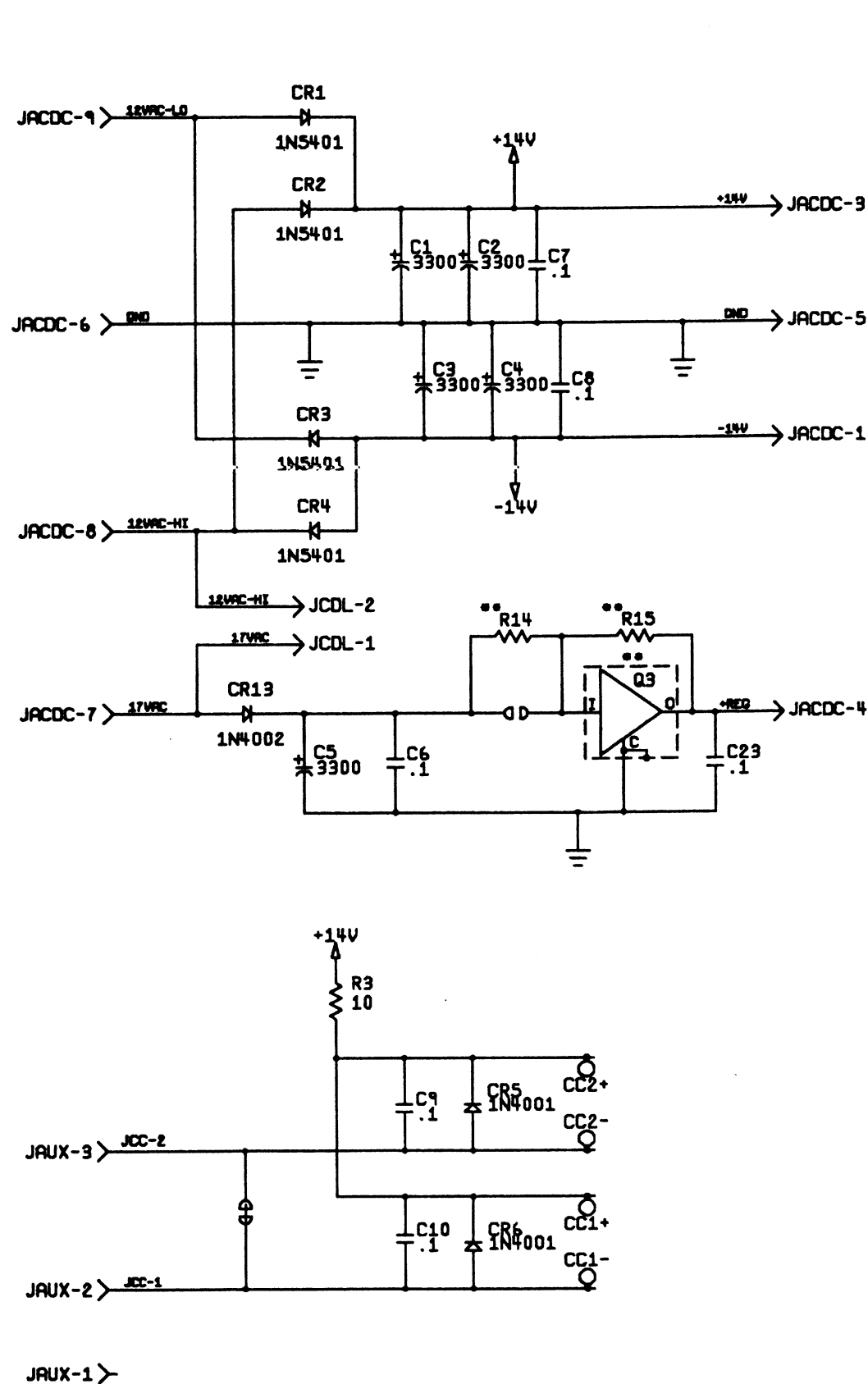




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720°™ Main Wiring Diagram



•• SEE TABLE BELOW FOR OPTIONAL ITEMS

DESIGNATION	VALUE	-01	-02
R1	10K POT	YES	YES
C17, C18	.22	YES	YES
C17-A, C18-A	.22	NO	NO
SW1	ON/OFF	YES	YES
Q3	SEE VER COL	LM7815	LM7812
R14	SEE VER COL	0 OHM	0 OHM
R15	0	NO	NO

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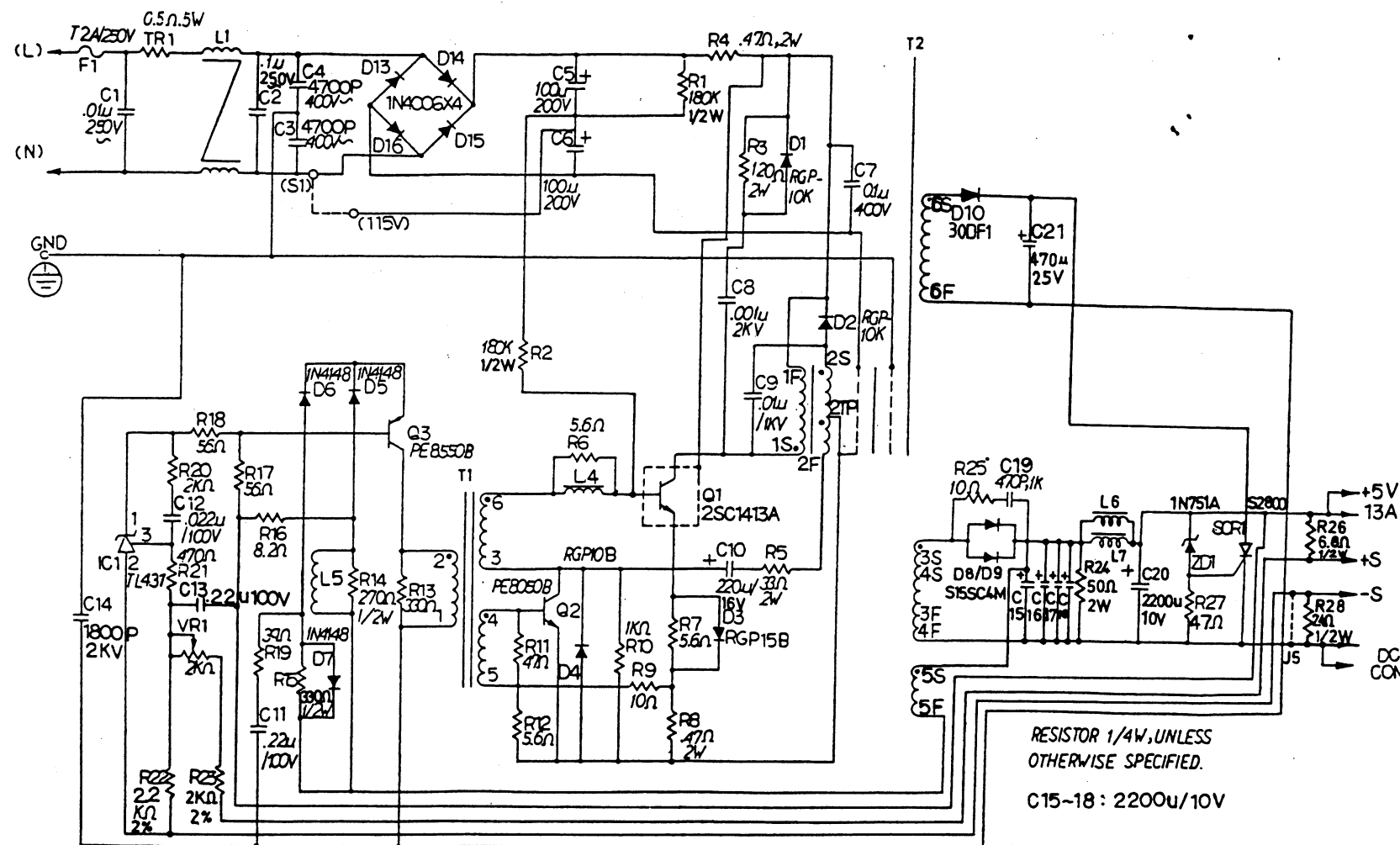
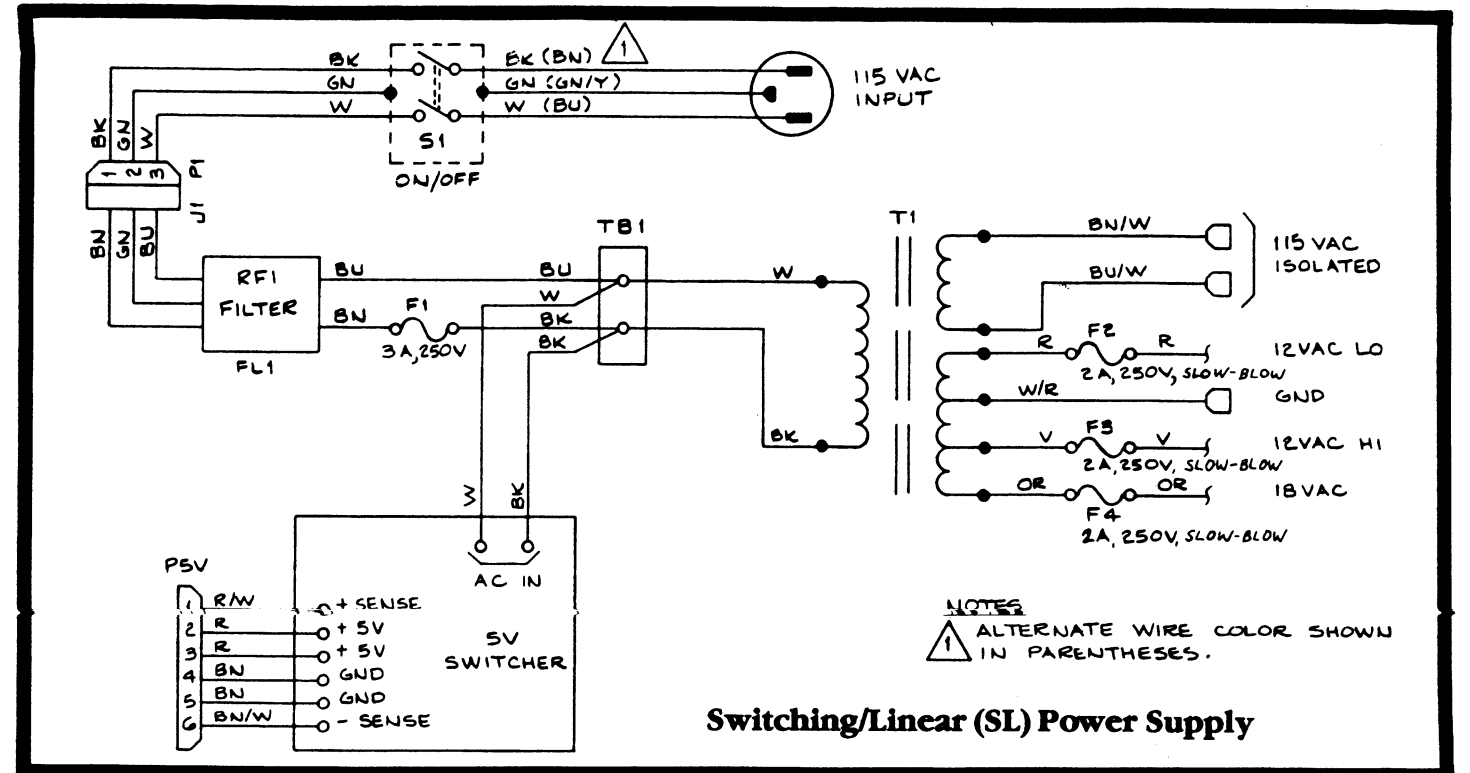
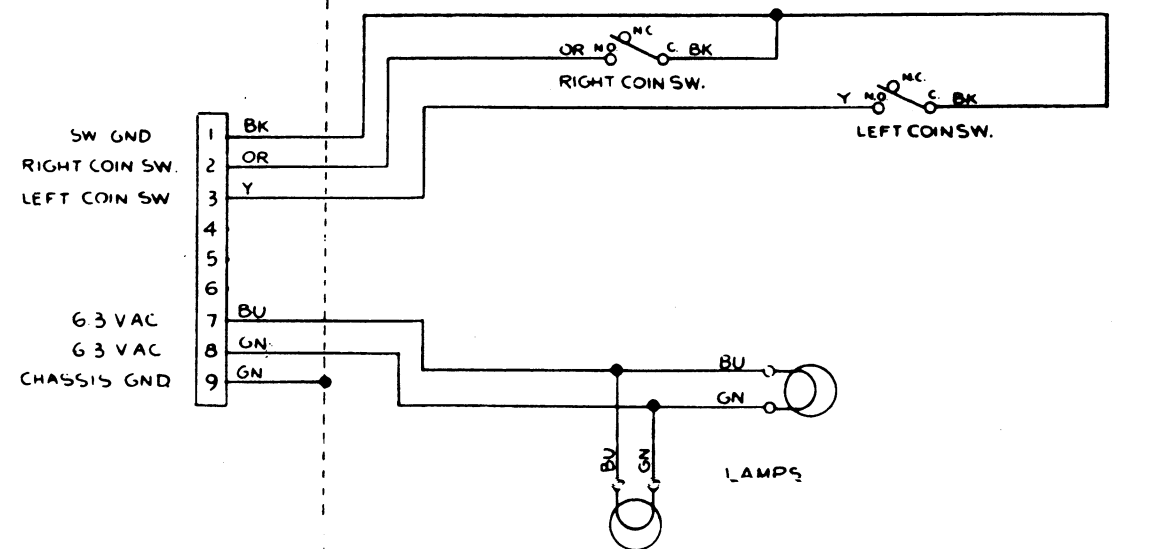


720°™ Audio II PCB Schematic Diagram

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Coin Door Wiring Diagram



RESISTOR 1/4W, UNLESS OTHERWISE SPECIFIED.
C15-18: 2200u/10V

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(SL) Power Supply, Coin Door, and 5V, 13A Power Supply Wiring Diagrams

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Main Microprocessor (T-11) Memory Map

Octal	Address Bus Signal Lines																R/W	Data Bus Signal Lines																Function and Size
	A A A A A A A A A A A A A A A A																	D D D D D D D D D D D D D D D D																
	1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0																	1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0																
5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0																		
000000-007777	0 0 0 0 A A A A A A A A A A A A																R/W	D D D D D D D D D D D D D D D D																Program RAM (4KB)
010000-010436	0 0 0 1 0 0 A A A A A A A A A 0																W	D D D D D D D D D D D D D D D D																Color RAM (144W)
"	0 0 0 1 0 0 A A A A A A A A A 0																W	D D D D																Z (Intensity)
"	0 0 0 1 0 0 A A A A A A A A A 0																W	D D D D																Blue
"	0 0 0 1 0 0 A A A A A A A A A 0																W	D D D D																Green
"	0 0 0 1 0 0 A A A A A A A A A 0																W	D D D D																Red
010000-010176	0 0 0 1 0 0 0 0 A A A A A A A 0																W	D D D D D D D D D D D D D D D D																Motion Object Color RAM (64W)
010200-010276	0 0 0 1 0 0 0 1 A A A A A A A 0																W	D D D D D D D D D D D D D D D D																Alphanumeric Color RAM (16W)
010400-010776	0 0 0 1 0 0 1 0 0 0 A A A A A 0																W	D D D D D D D D D D D D D D D D																Playfield Color RAM (128W)
012000	0 0 0 1 0 1 0 0 0 0 0																W	D D D D D D D																Program Page 0 Address
012002	0 0 0 1 0 1 0 0 0 0 1																W	D D D D D D D																Program Page 1 Address
012200	0 0 0 1 0 1 0 0 1 0 0																W																	A/D Converter Start Strobe
012000-012002	0 0 0 1 0 1 0 0 A																R	D D D D D D D D D D																A/D Converter Output
012400	0 0 0 1 0 1 0 1 0 1 0																W	D D																Video Memory Page Select (VMMU)
012600	0 0 0 1 0 1 0 1 0 1 1 0 0																W																	IRQ0 Clear
012640	0 0 0 1 0 1 0 1 0 1 1 0 1																W																	6502 Reset
012700	0 0 0 1 0 1 0 1 0 1 1 1 0																W																	IRQ2 Clear
012740	0 0 0 1 0 1 0 1 0 1 1 1 1																W																	IRQ3 Clear
013000	0 0 0 1 0 1 1 0 0 0 0																W	D																IRQ0 Enable 6502 RD (Active High)
013000	0 0 0 1 0 1 1 0 0 0 0																W	D																IRQ1 Enable 6502 WT (Active High)
013000	0 0 0 1 0 1 1 0 0 0 0																W	D																IRQ2 Enable 32V (Active High)
013000	0 0 0 1 0 1 1 0 0 0 0																W	D																IRQ3 Enable VBLANK (Active High)
013200	0 0 0 1 0 1 1 0 1 0 0																W	D D D D D D D D D D																Communications Port Write
013400	0 0 0 1 0 1 1 1 0 0 0																W	D D D D D D D D D D D D D D D D																Horizontal Scroll & PF Bank 0
013600	0 0 0 1 0 1 1 1 1 0 0																W	D D D D D D D D D D D D D D D D																Vertical Scroll & PF Bank 1
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																SW 6 (Active Low)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																SW 5 (Active Low)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																SW 4 (Active Low)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																SW 3 (Active Low)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																6502 Comm. Flag (Active High)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																T-11 Comm. Flag (Active High)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																SW 2 (Active Low)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																SW 1 (Active Low)
014000	0 0 0 1 1 0 0 0 0 0 0																R	D																Self-Test (Active Low)
016000	0 0 0 1 1 1 0 0 0 0 0																R	D D D D D D D D D D																Communications Port Read
020000-033776	0 0 1 A A A A A A A A A A A A A 0																R/W	D D D D D D D D D D D D D D D D																Alphanumerics RAM (VMMU=0) (3KW)
"	0 0 1 A A A A A A A A A A A A A 0																R/W	D D D D D D D D D D D D D D D D																ANPIC
034000-037776	0 0 1 1 1 A A A A A A A A A A A 0																R/W	D D D D D D D D D D D D D D D D																Motion Object RAM (VMMU=0) (1KW)
"	0 0 1 1 1 A A A A A A A A A A 0 0 0																R/W	D D D D D D D D D D D D D D D D																MOV
"	0 0 1 1 1 A A A A A A A A A A 0 1 0																R/W	D D D D D D D D D D D D D D D D																MOPIC
"	0 0 1 1 1 A A A A A A A A A A 1 0 0																R/W	D D D D D D D D D D D D D D D D																MOH
"	0 0 1 1 1 A A A A A A A A A A 1 1 0																R/W	D D D D D D D D D D D D D D D D																MOLNK
020000-037776	0 0 1 A A A A A A A A A A A A A 0																R/W	D D D D D D D D D D D D D D D D																Playfield RAM Top (VMMU=2) (4KW)
020000-037776	0 0 1 A A A A A A A A A A A A A 0																R/W	D D D D D D D D D D D D D D D D																Playfield RAM Bottom (VMMU=3) (4KW)
040000-057776	0 1 0 A A A A A A A A A A A A A 0																R	D D D D D D D D D D D D D D D D																Paged Program (Page 0) (4KW)
060000-077776	0 1 1 A A A A A A A A A A A A A 0																R	D D D D D D D D D D D D D D D D																Paged Program (Page 1) (4KW)
100000-177776	1 A A A A A A A A A A A A A A A 0																R	D D D D D D D D D D D D D D D D																Program ROM (16KW)

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720°™ Main Microprocessor Memory Map

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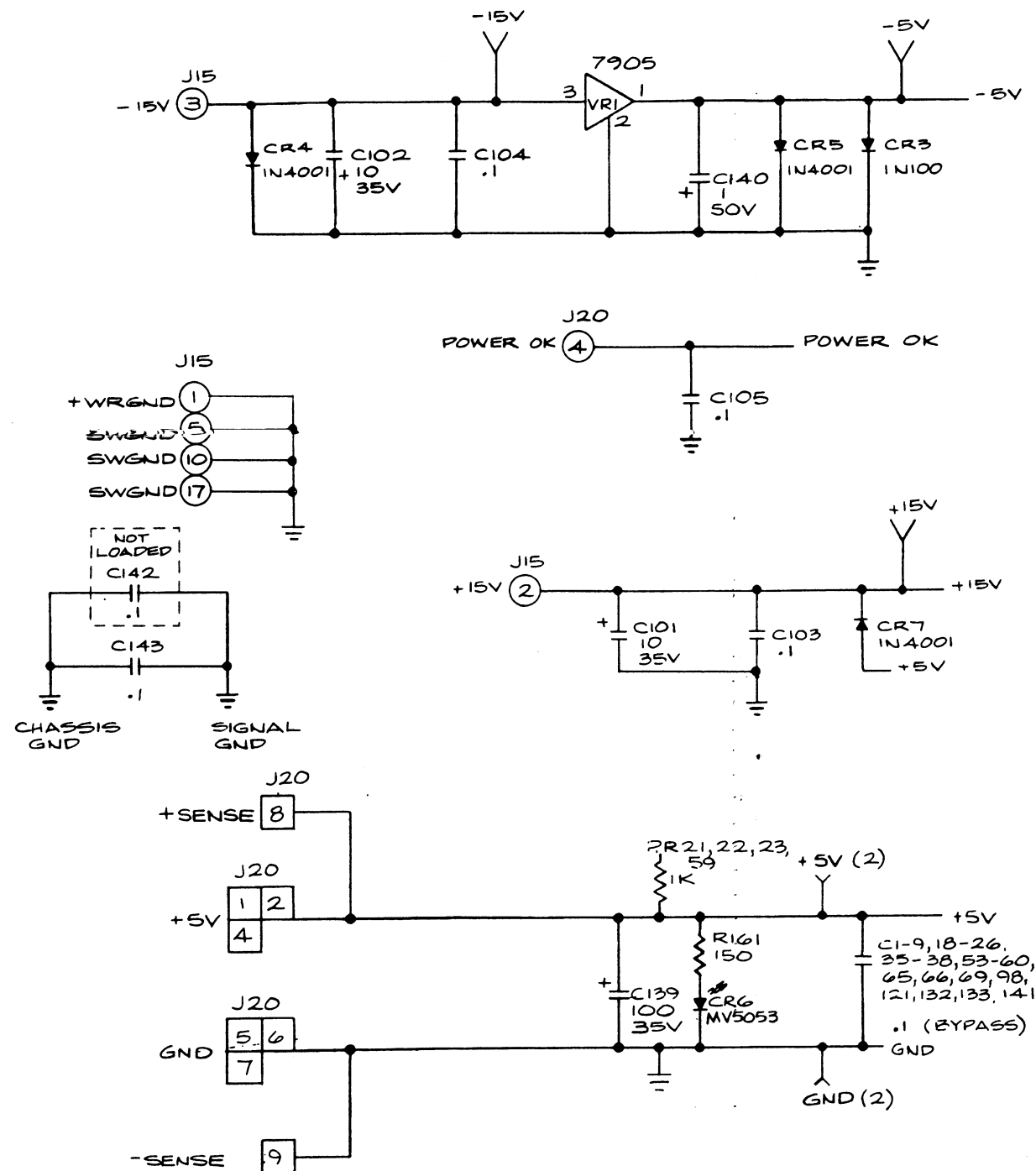
Sound Microprocessor (6502) Memory Map

Hexa- decimal	A A A A A A A A A A A A A A A A		D D D D D D D D	
	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R/W	0 0 0 0 0 0 0 0	
	5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0		7 6 5 4 3 2 1 0	Function and Size
0000-0FFF	0 0 0 0 A A A A A A A A A A A A	R/W	D D D D D D D D	Program RAM (4KB)
1000-17FF	0 0 0 1 0 A A A A A A A A A A A A	R/W	D D D D D D D D	EEROM (2KB)
1800-180F	0 0 1 1 0 0 0 A A A A A A A A A A	R/W	D D D D D D D D	POKEY 1 (16B)
1810-1813	0 0 1 1 0 0 1 A A A A A A A A A A	R	D D D D D D D D	LETA
1830-183F	0 0 1 1 0 1 1 A A A A A A A A A A	R/W	D D D D D D D D	POKEY 2 (16B)
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	T-11 Talk (Active High)
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	6502 Talk (Active High)
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	TI READY (Active High)
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	Self-Test Switch (Active Low)
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	Auxiliary Coin Switch (Active Low)
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	Left Coin Switch (Active Low)
1840	0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0	R	D	Right Coin Switch (Active Low)
1850-1851	0 0 1 1 1 0 1 0 0 0 0 0 0 0 0 0	R	D D D D D D D D	Yamaha Sound Chip
1860	0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0	R	D D D D D D D D	Communications Port Read
1870	0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0	W	D D D D D D D D	TI Data
1872-1873	0 0 1 1 1 1 1 0 0 0 1 A 0 0 0 0	W	D D D D D D D D	TI Write Enable
1874	0 0 1 1 1 1 1 0 1 0 0 0 0 0 0 0	W	D D D D D D D D	Communications Port Write
1876	0 0 1 1 1 1 1 0 1 1 0 0 0 0 0 0	W	D	Right Coin Counter (Active High)
1876	0 0 1 1 1 1 1 0 1 1 0 0 0 0 0 0	W	D	Left Coin Counter (Active High)
1878	0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0	W		IRQ Clear
187A	0 0 1 1 1 1 1 1 0 1 0 0 0 0 0 0	W	D D D	Yamaha Mixer
187A	0 0 1 1 1 1 1 1 0 1 0 0 0 0 0 0	W	D D	POKEY Mixer
187A	0 0 1 1 1 1 1 1 0 1 0 0 0 0 0 0	W	D D D	TI Sound Mixer
187C	0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0	W	D	LED 1
187C	0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0	W	D	LED 2
187C	0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0	W	D	LETA Resolution
187C	0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0	W	D	TI Frequency Select
187E	0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0	W	D	Sound Enable (Active High)
4000-7FFF	0 1 A A A A A A A A A A A A A A A A	R	D D D D D D D D	Program ROM (16KB)
8000-FFFF	1 A A A A A A A A A A A A A A A A	R	D D D D D D D D	Program ROM (32KB)

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720°™ Sound
Microprocessor Memory Map



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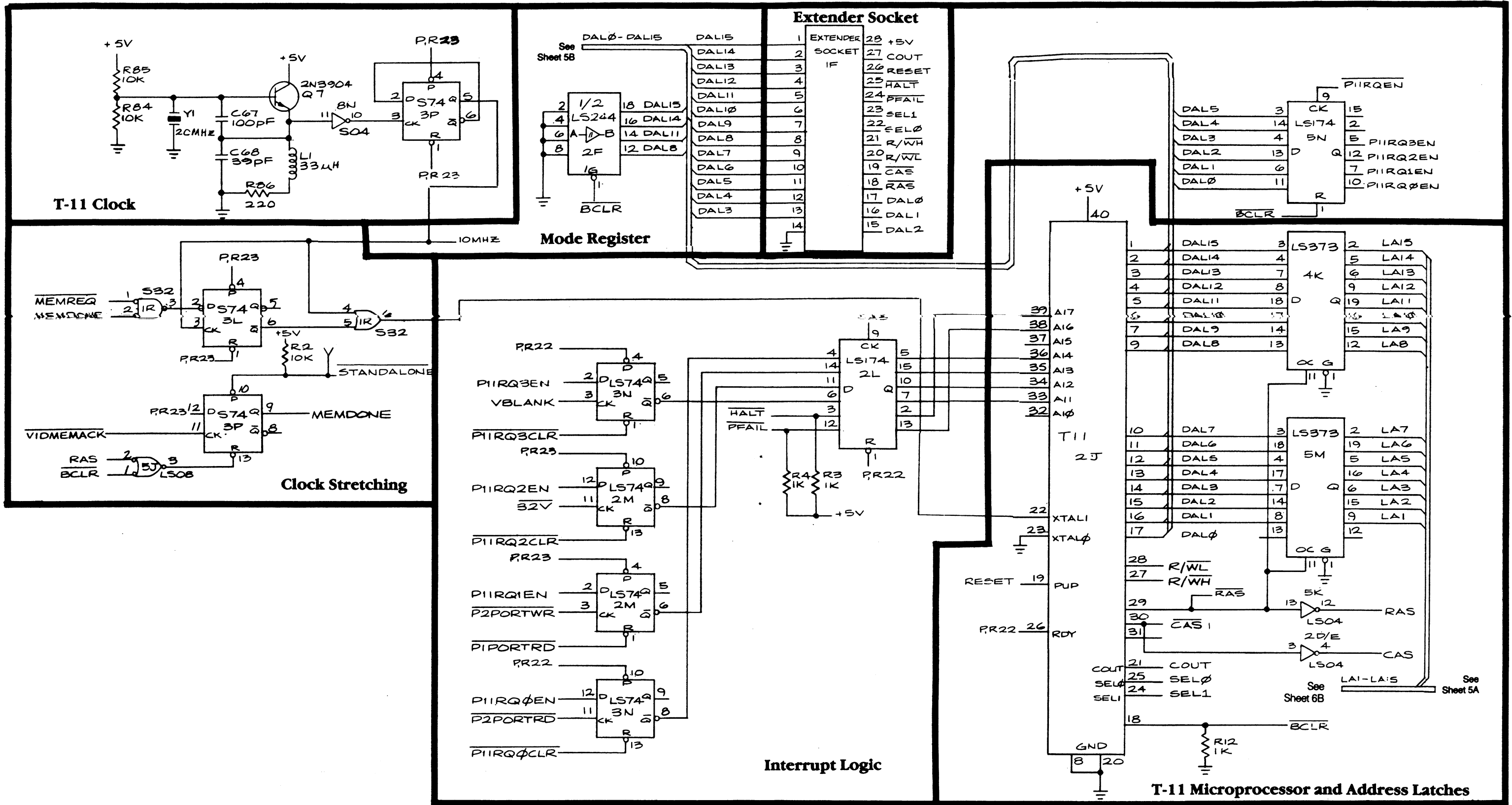
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720°™ CPU PCB Schematic Diagram

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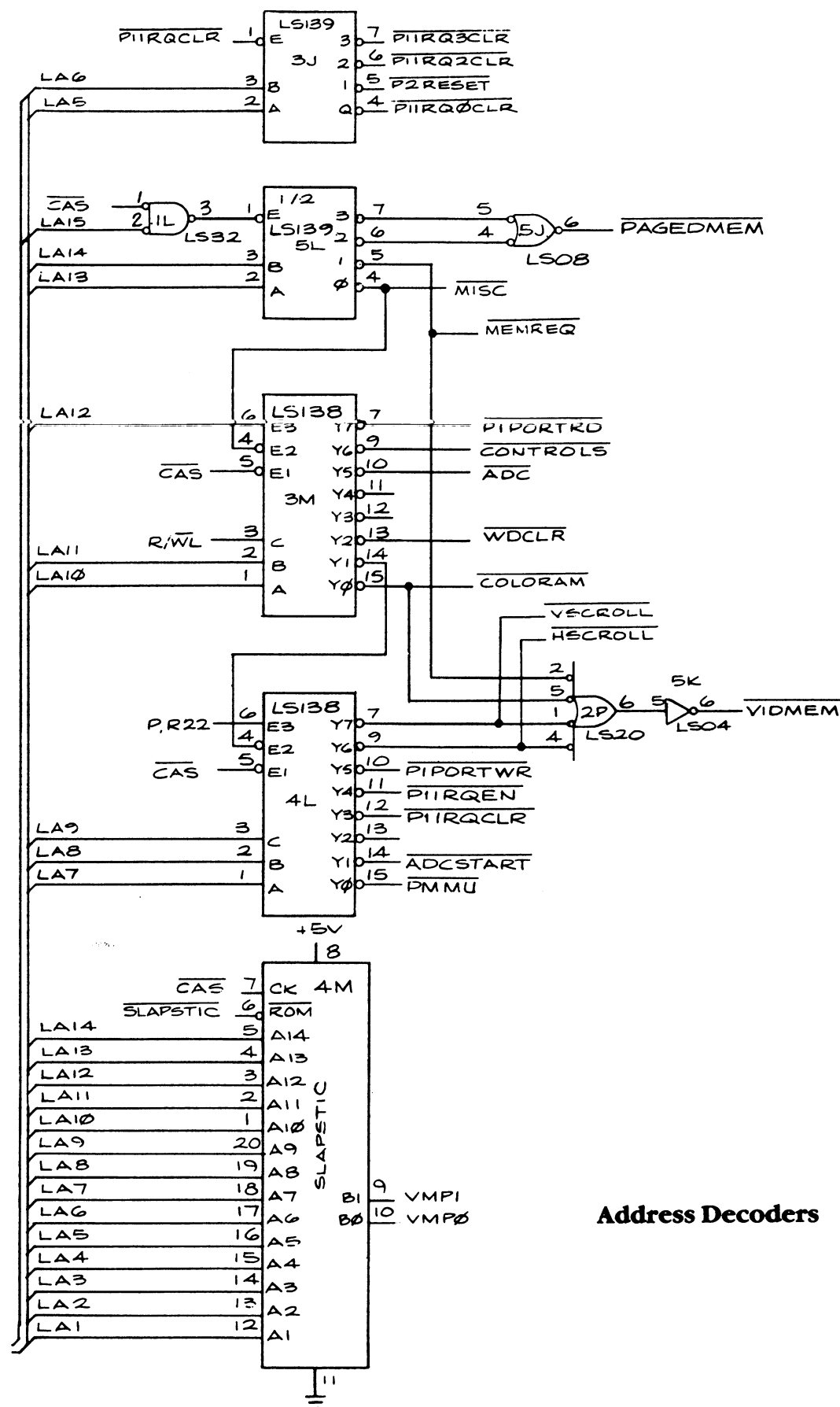
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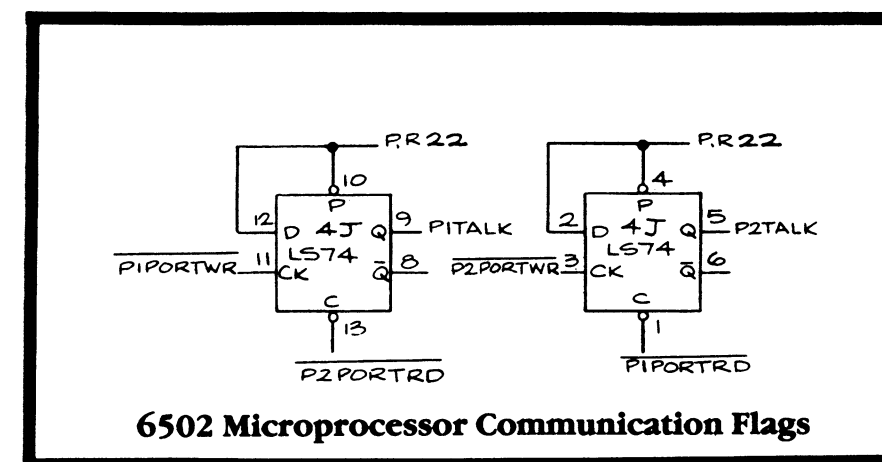
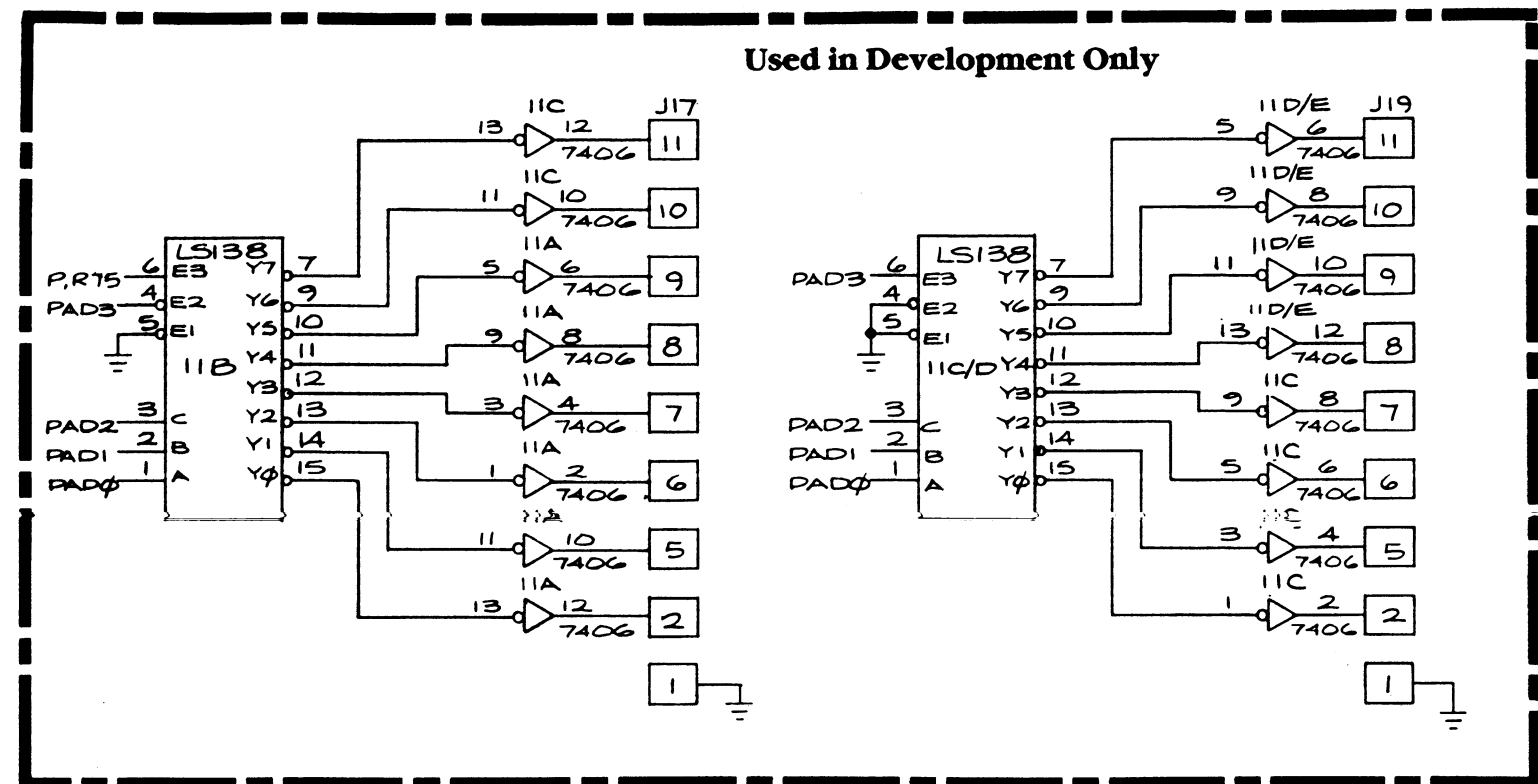
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**720[™] CPU PCB
Schematic Diagram**



Address Decoders



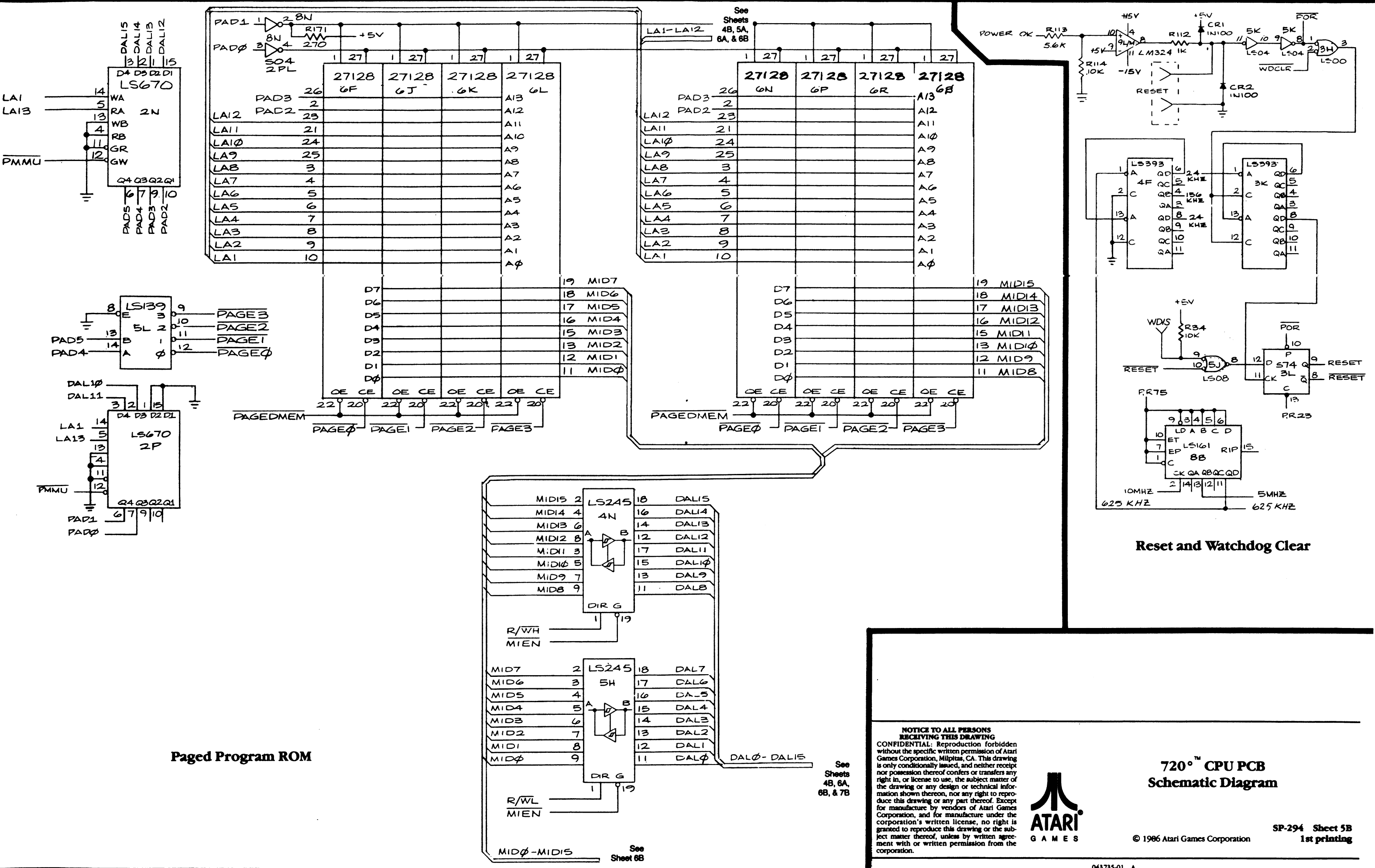
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7200™ CPU PCB Schematic Diagram

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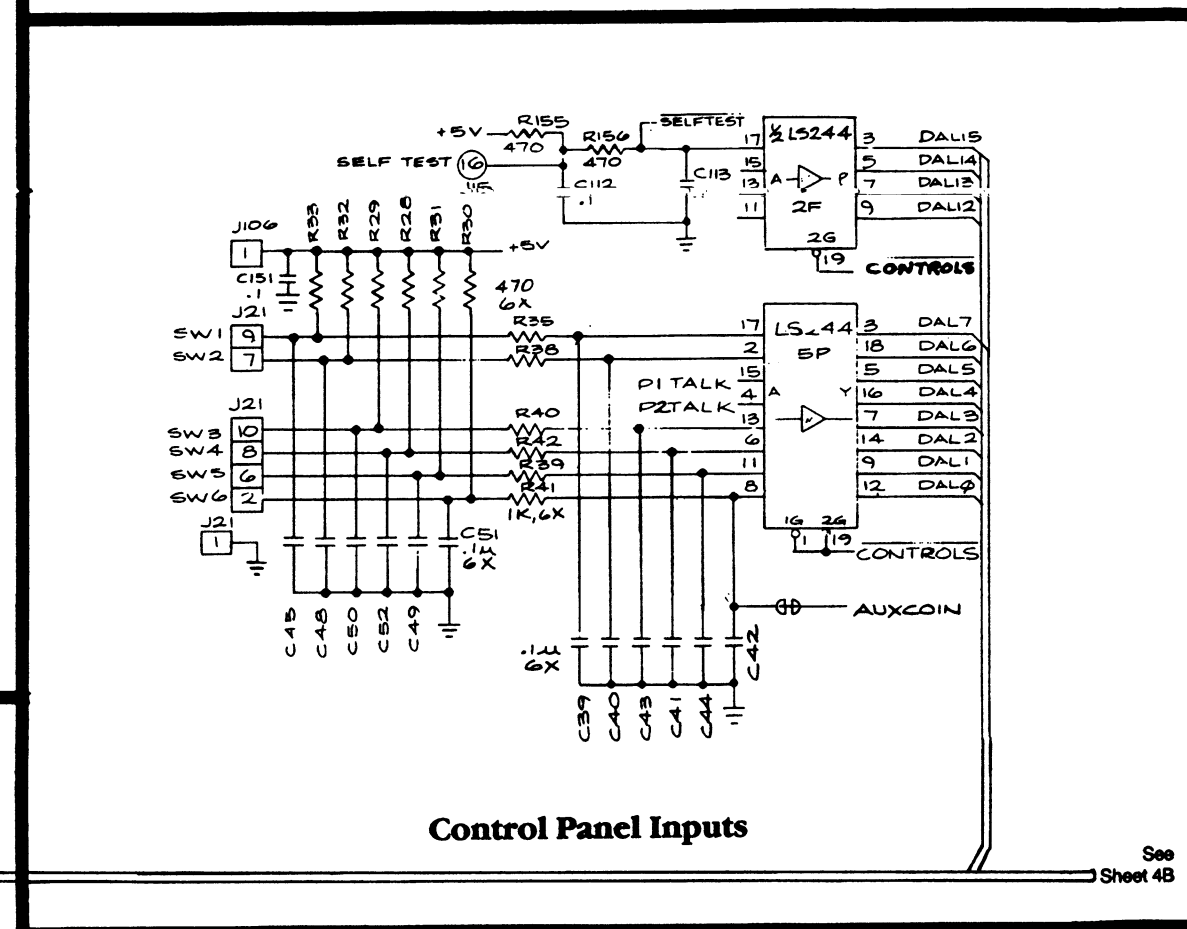
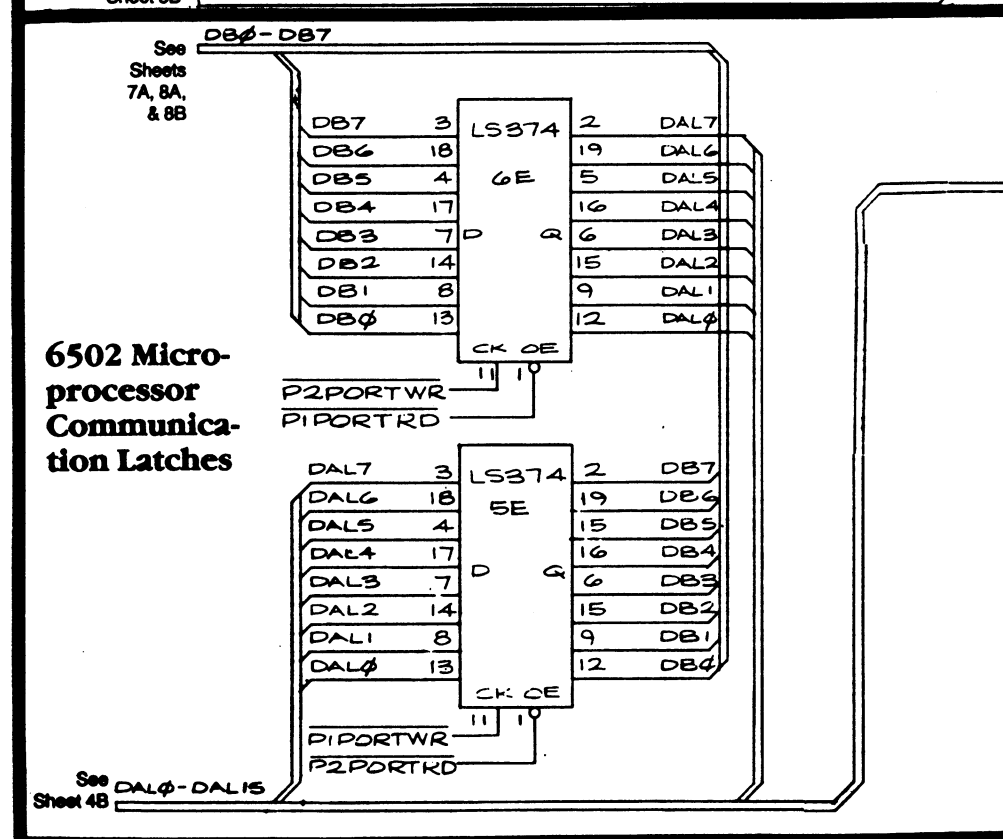
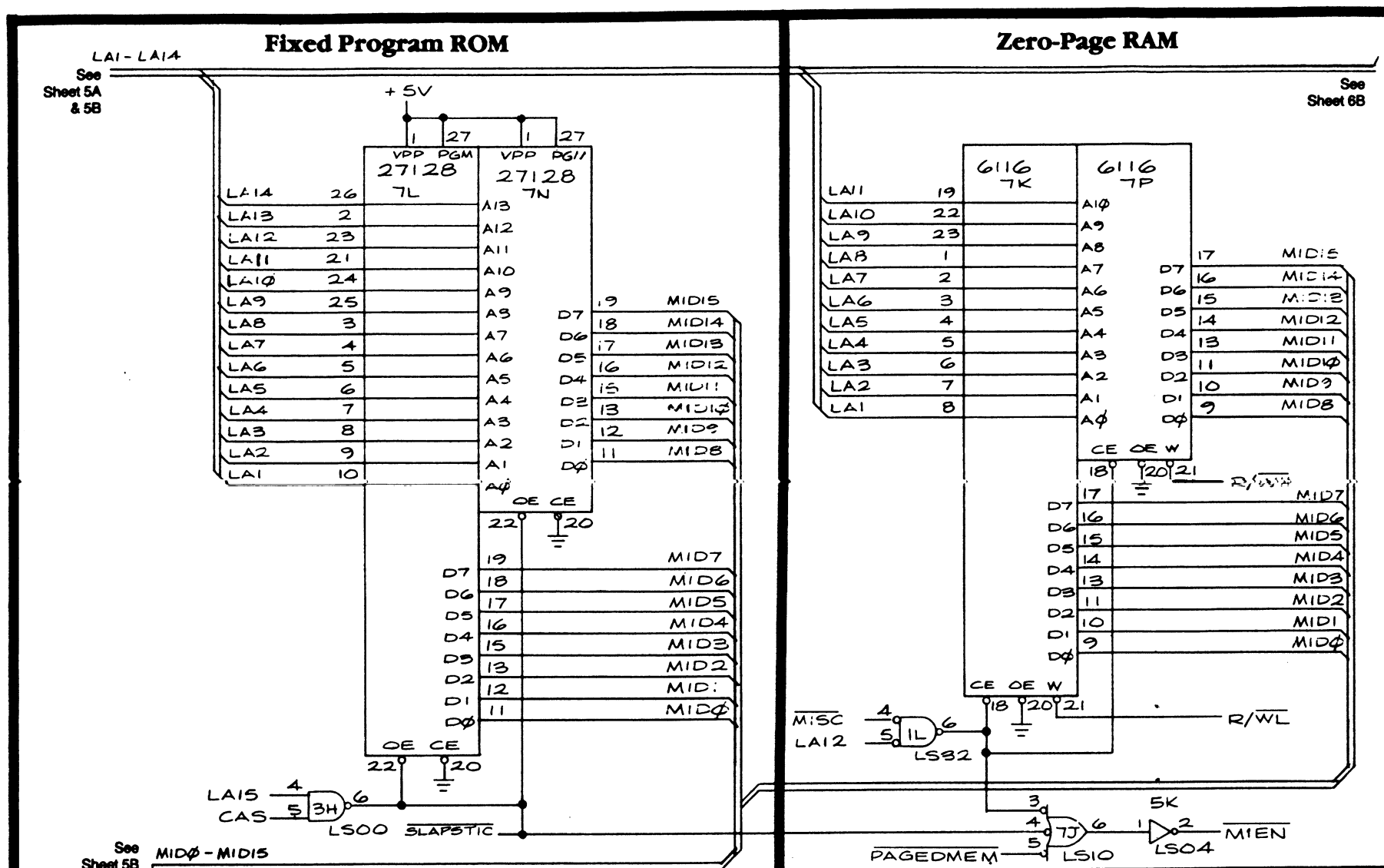
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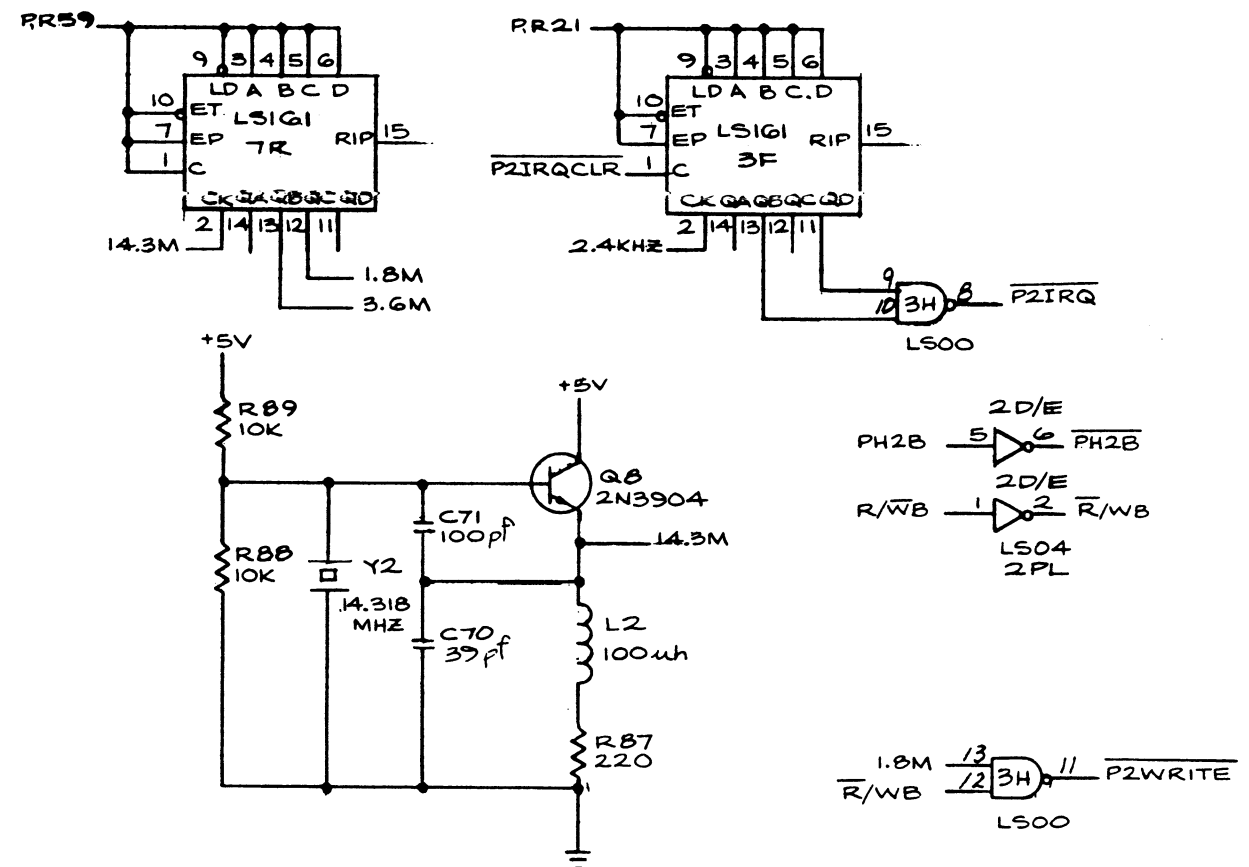
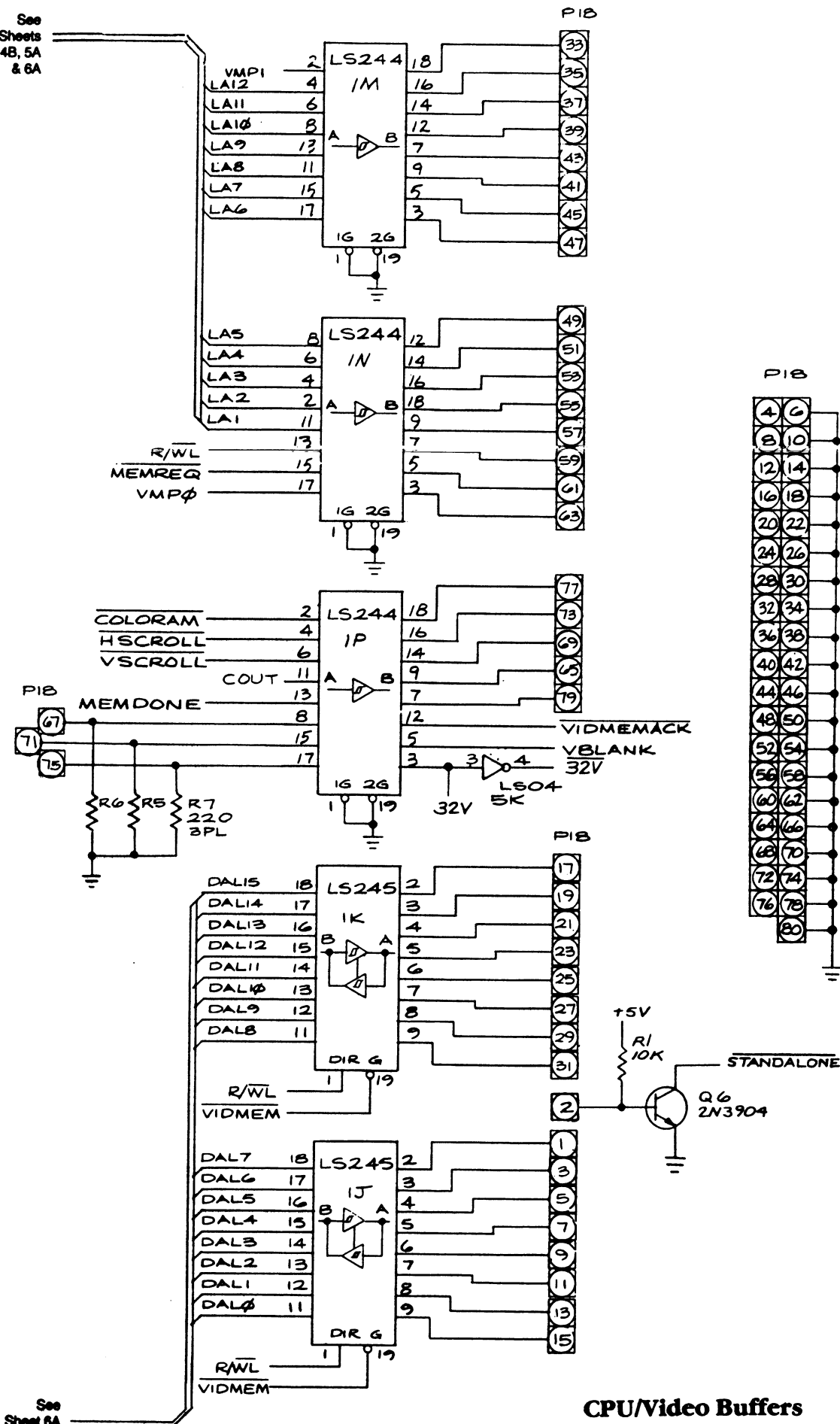
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720° CPU PCB Schematic Diagram



See
Sheets
4B, 5A
& 6A



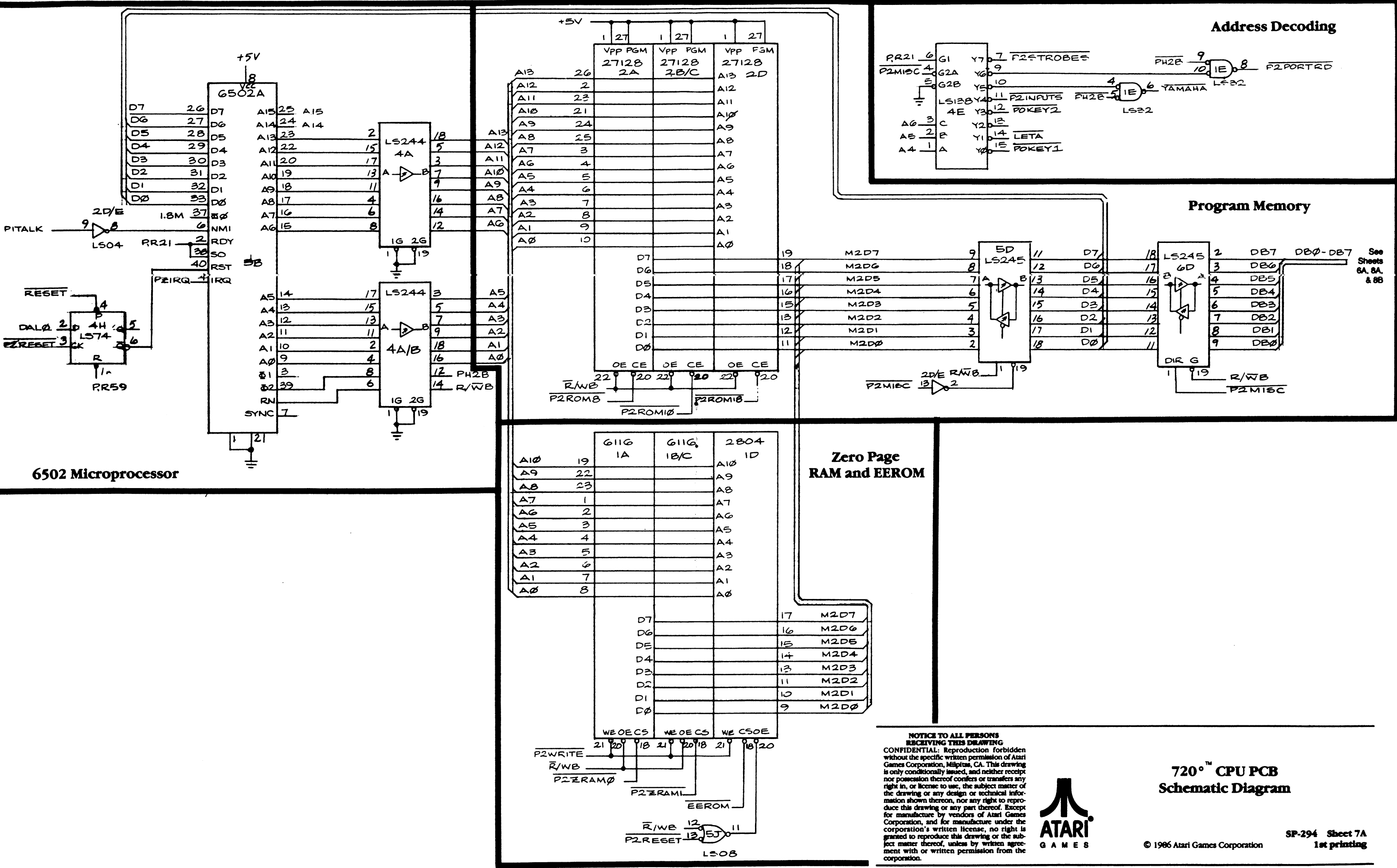
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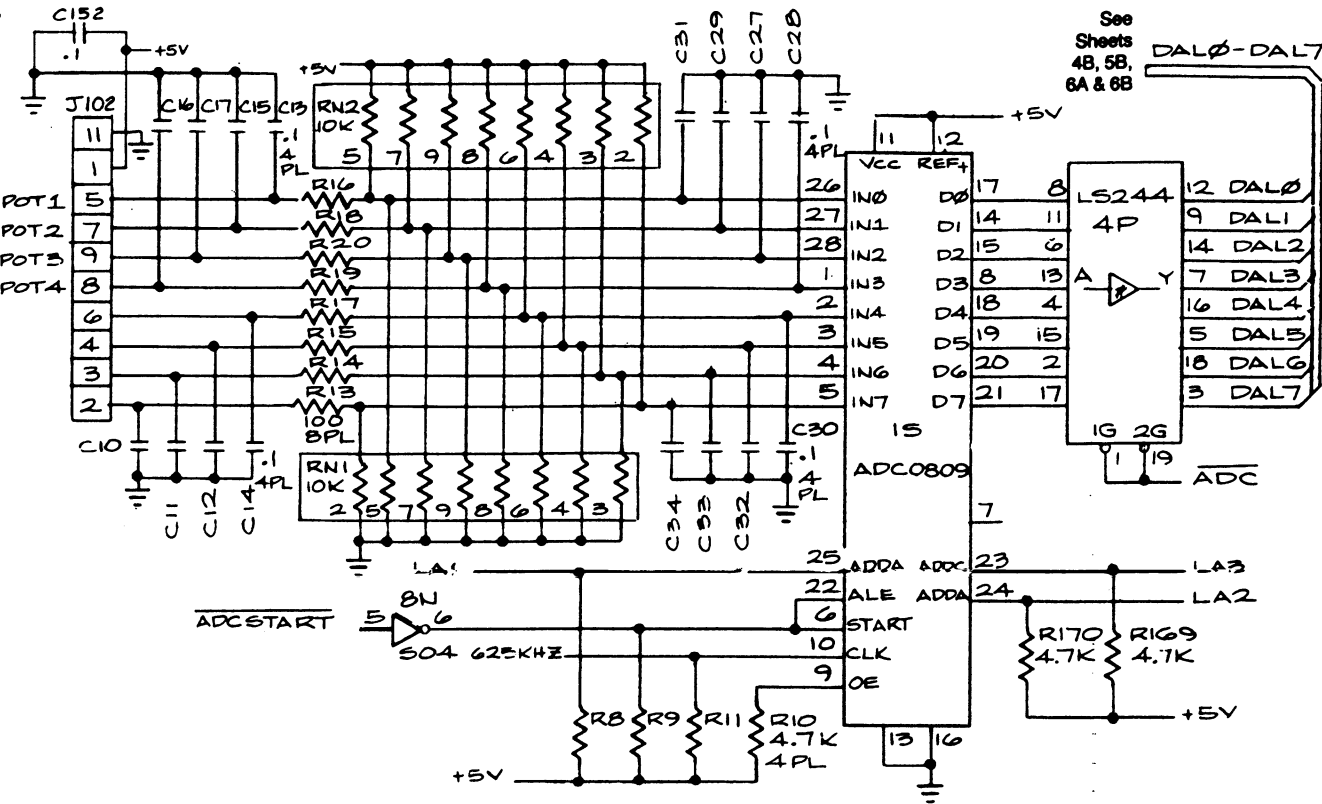
720°™ CPU PCB Schematic Diagram

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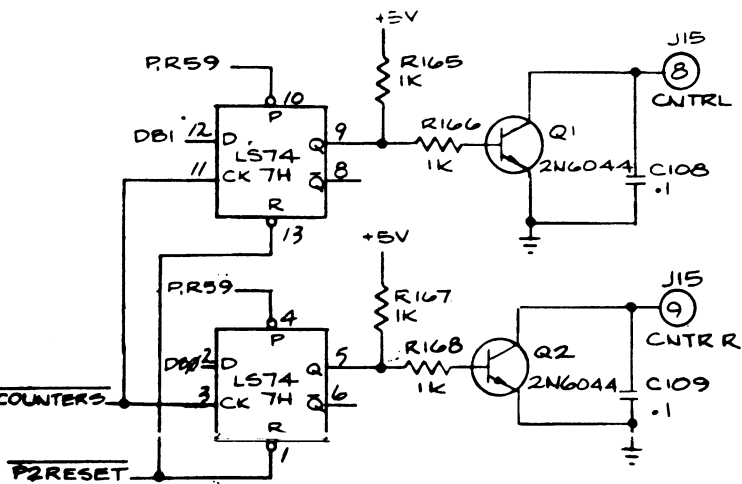
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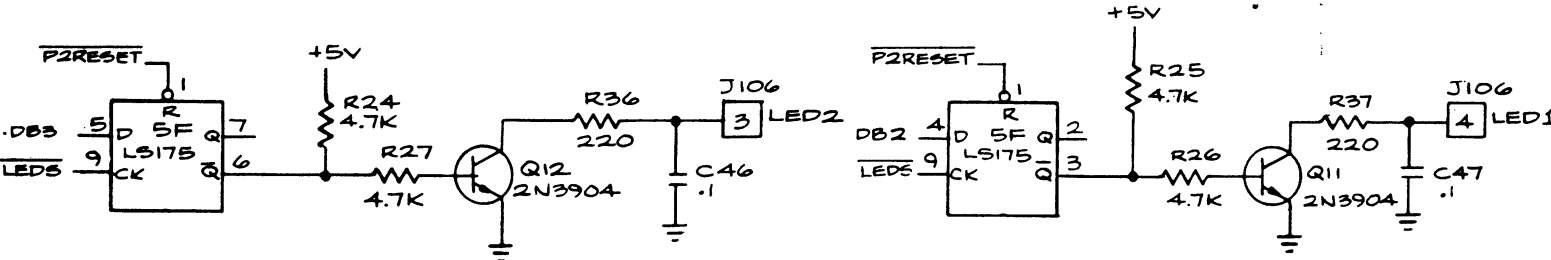
A/D Converter



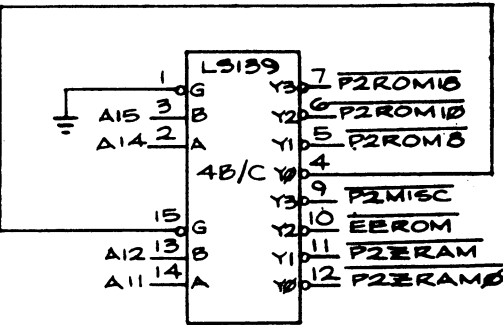
Coin Counters



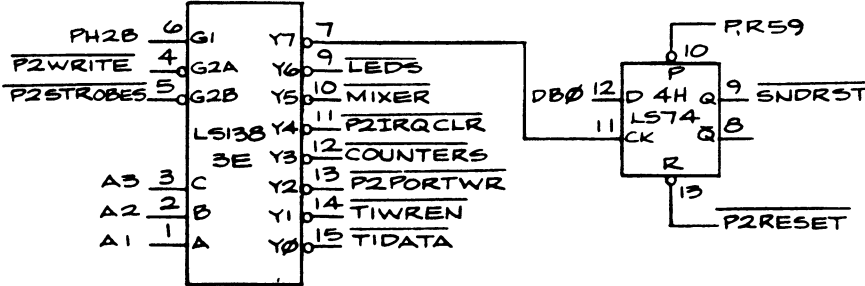
LED Drivers



Address Decoding



Address Decoding



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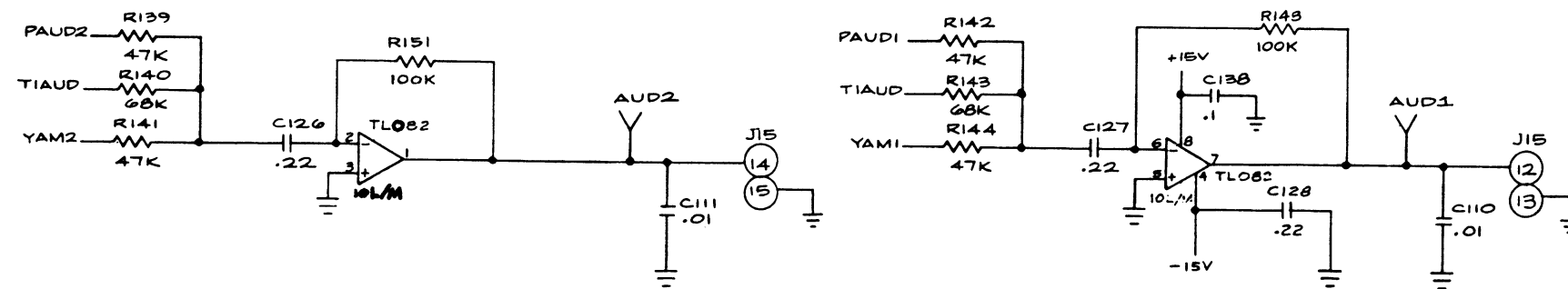
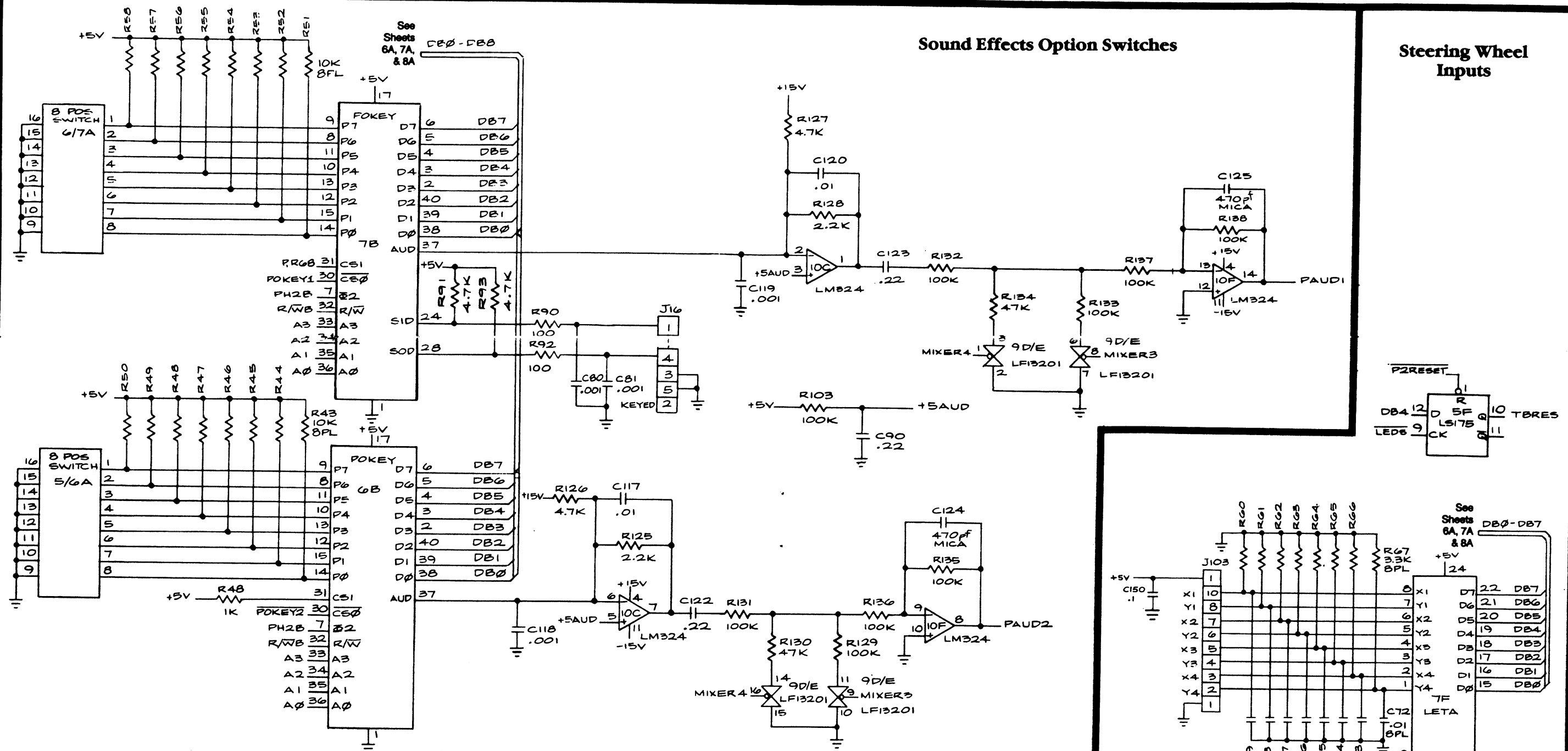
720° CPU PCB
Schematic Diagram

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Sound Effects Option Switches

Steering Wheel Inputs



Audio Output Drivers

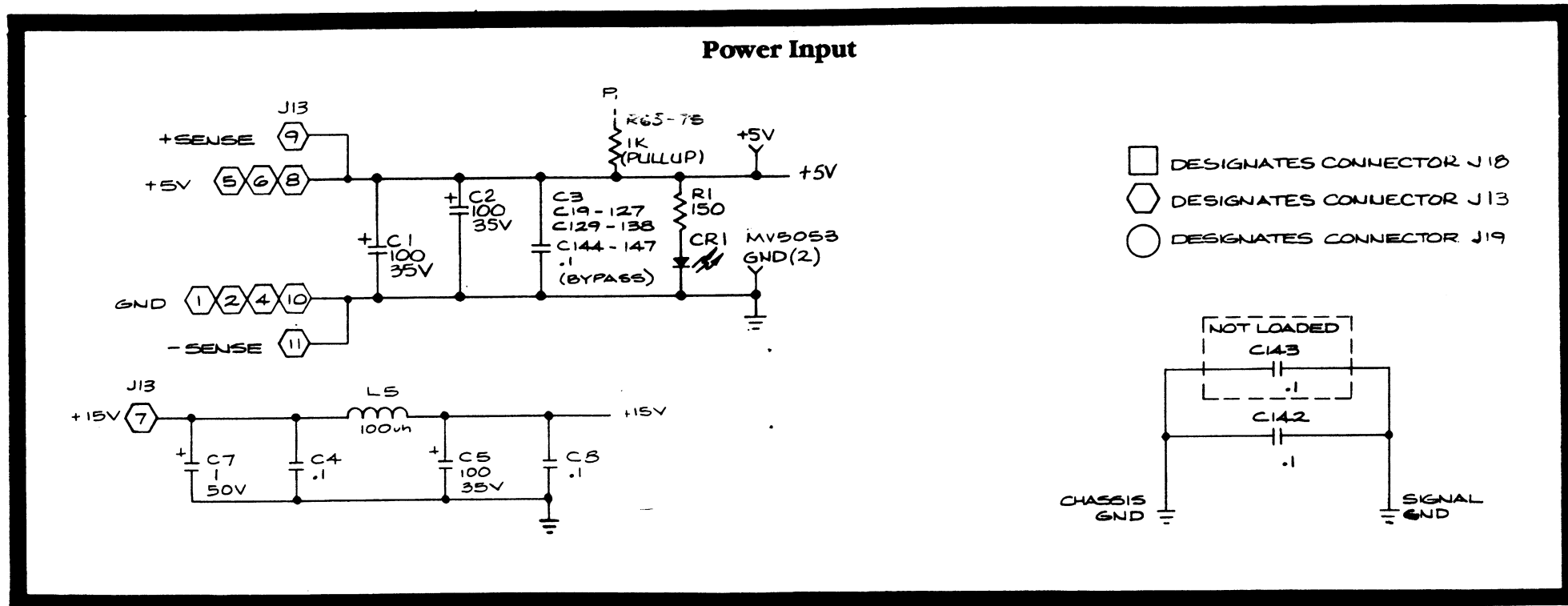
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720° CPU PCB Schematic Diagram

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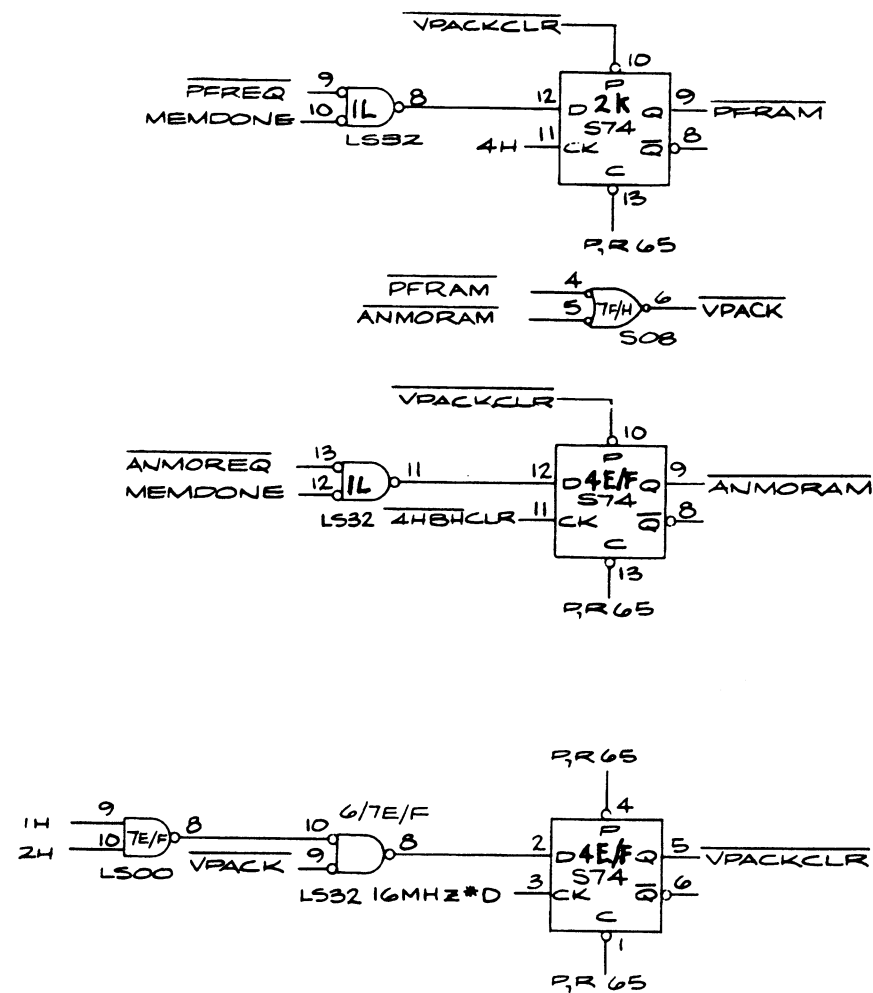


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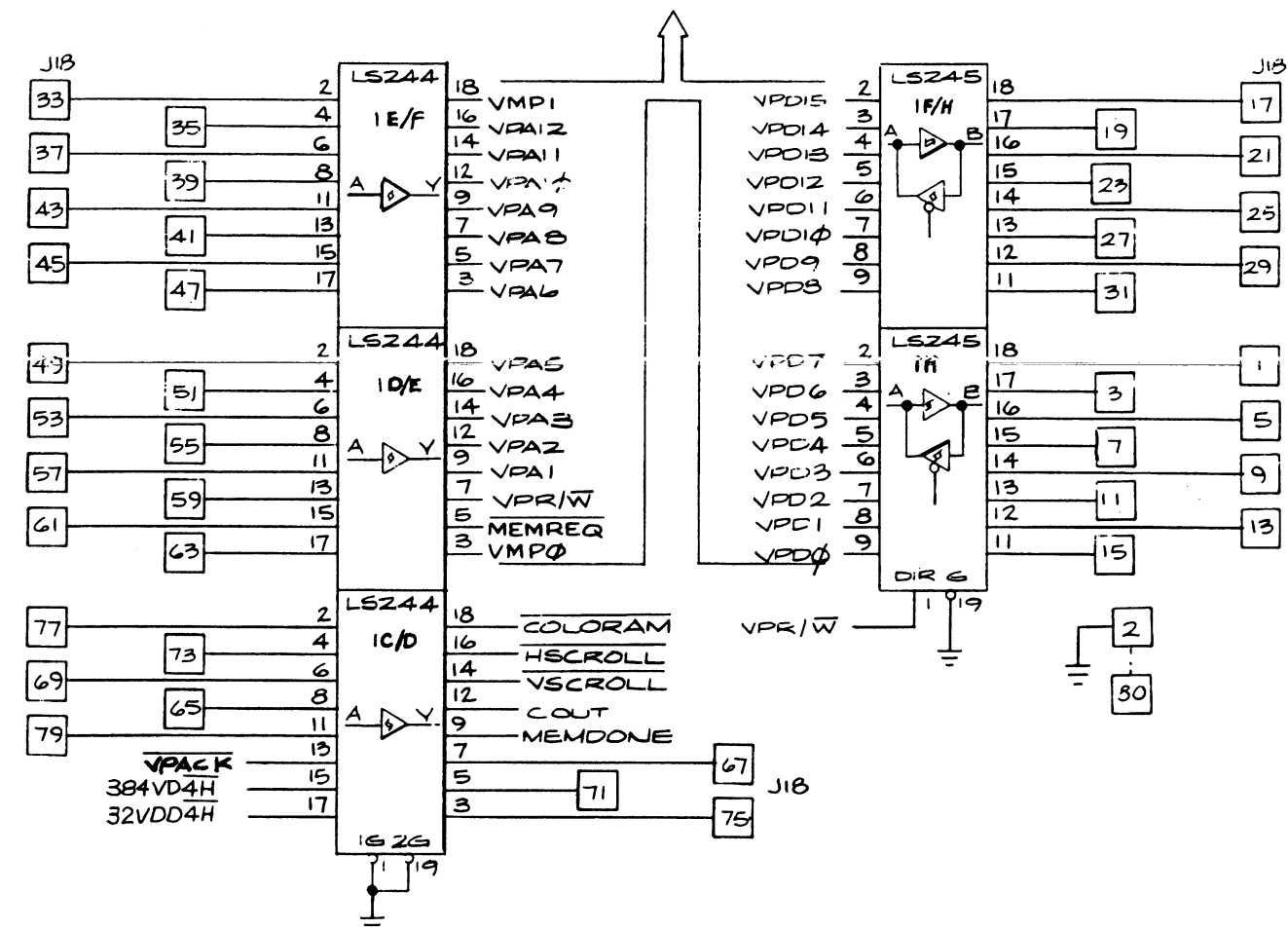
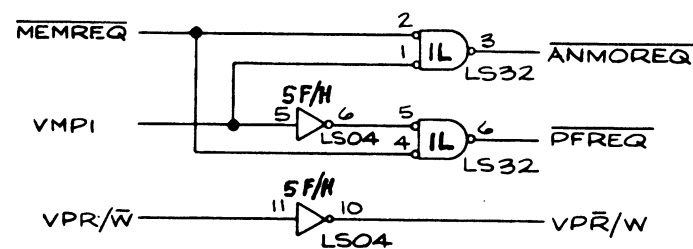
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720°™ Video PCB Schematic Diagram



Address Decoding Control Signals



Video/CPU Buffers

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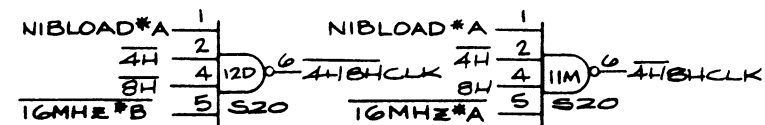
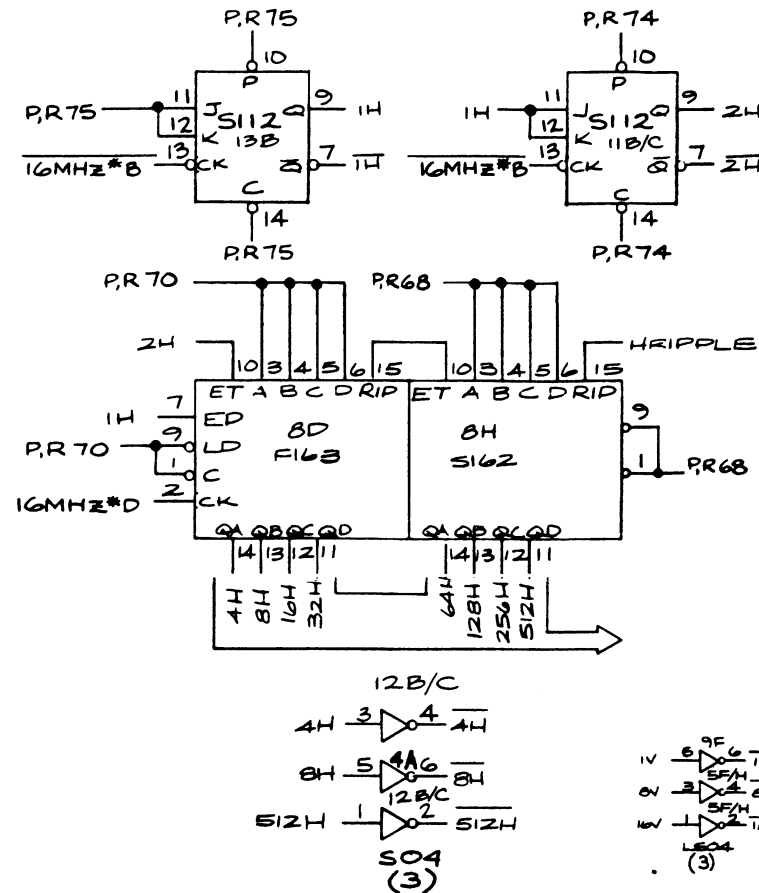
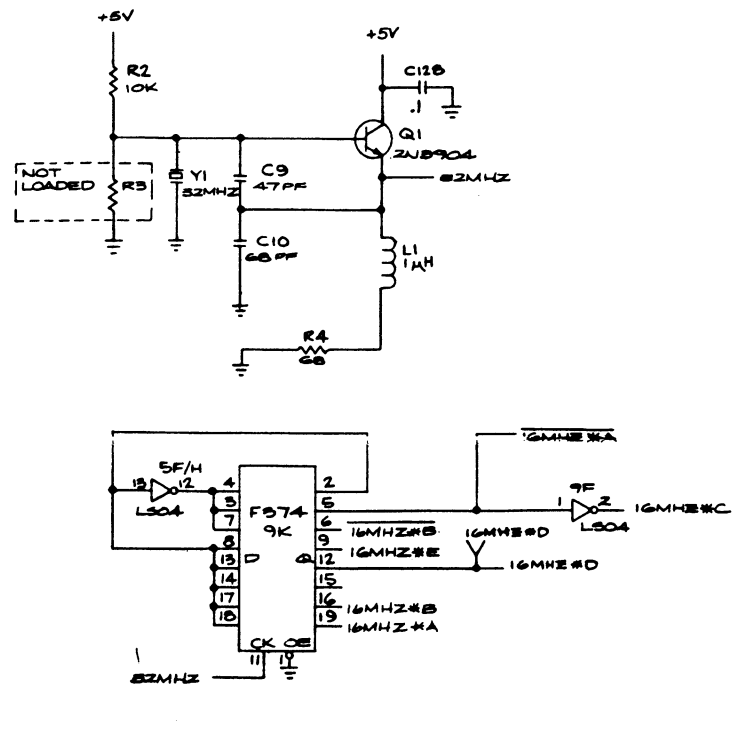


720^o™ Video PCB
 Schematic Diagram

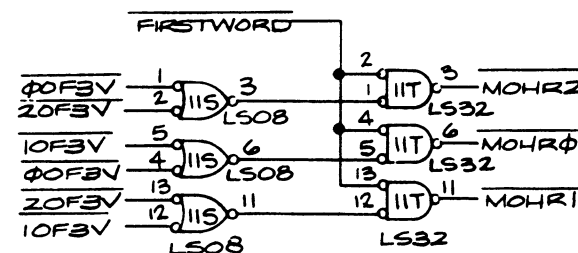
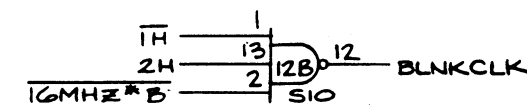
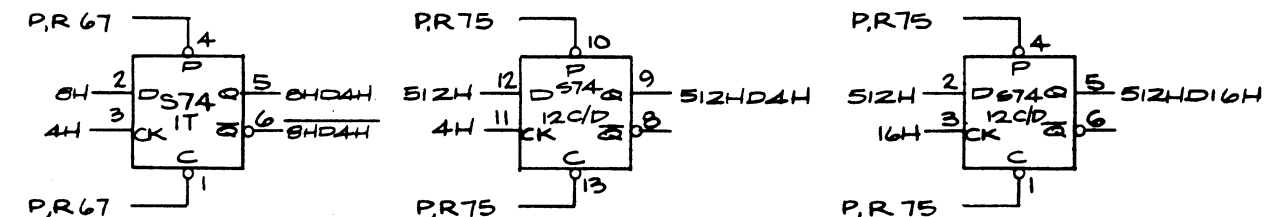
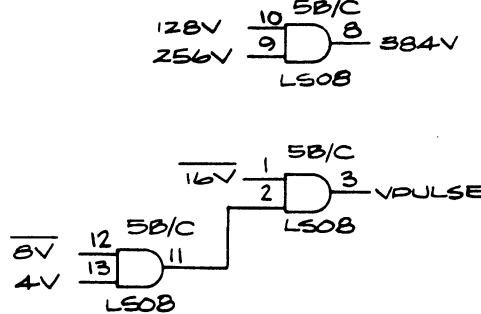
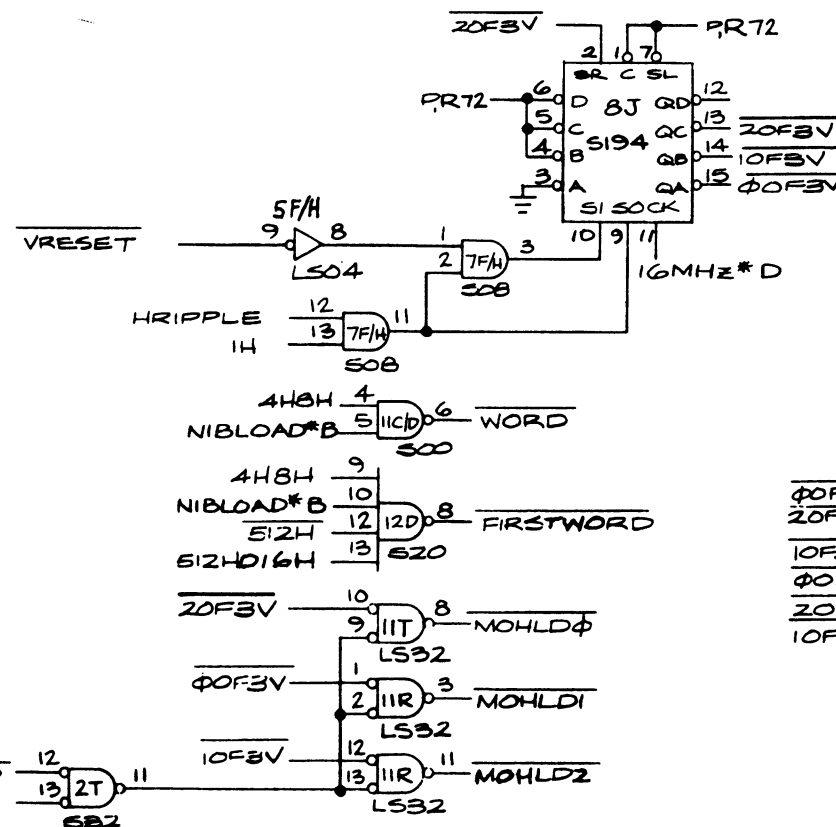
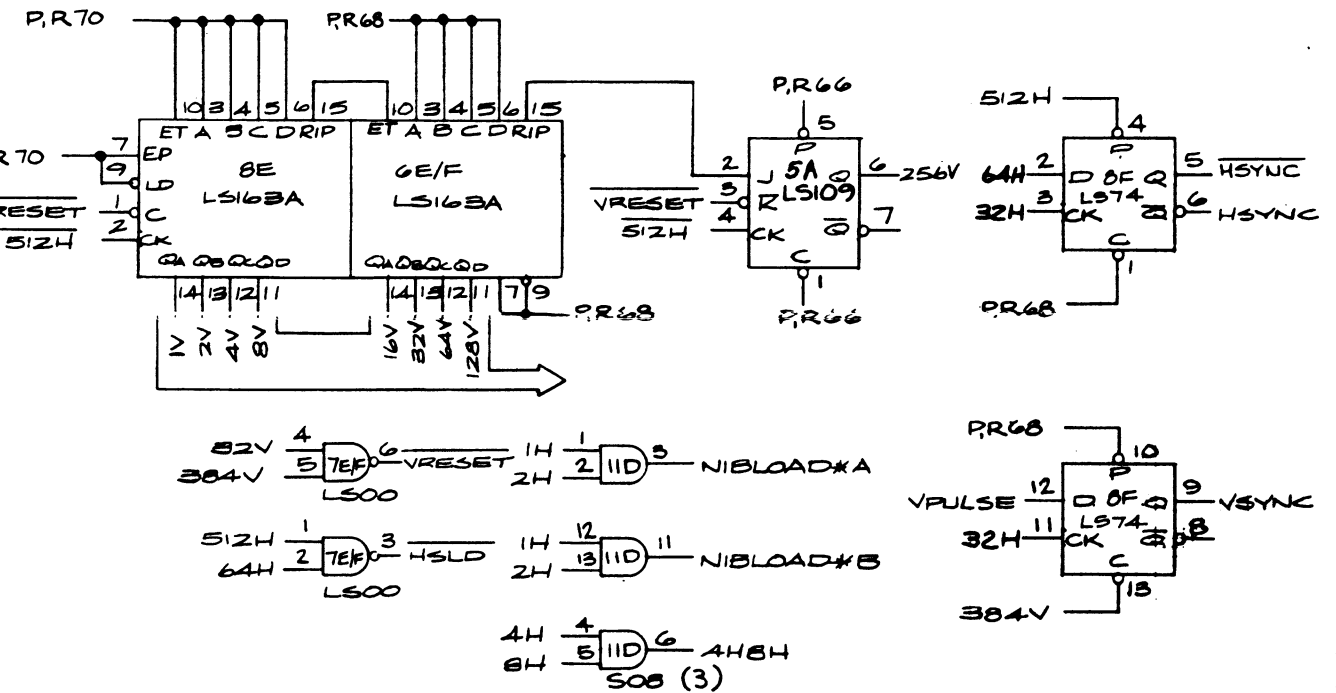
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Video Clock



Sync Chain and Timing Strokes



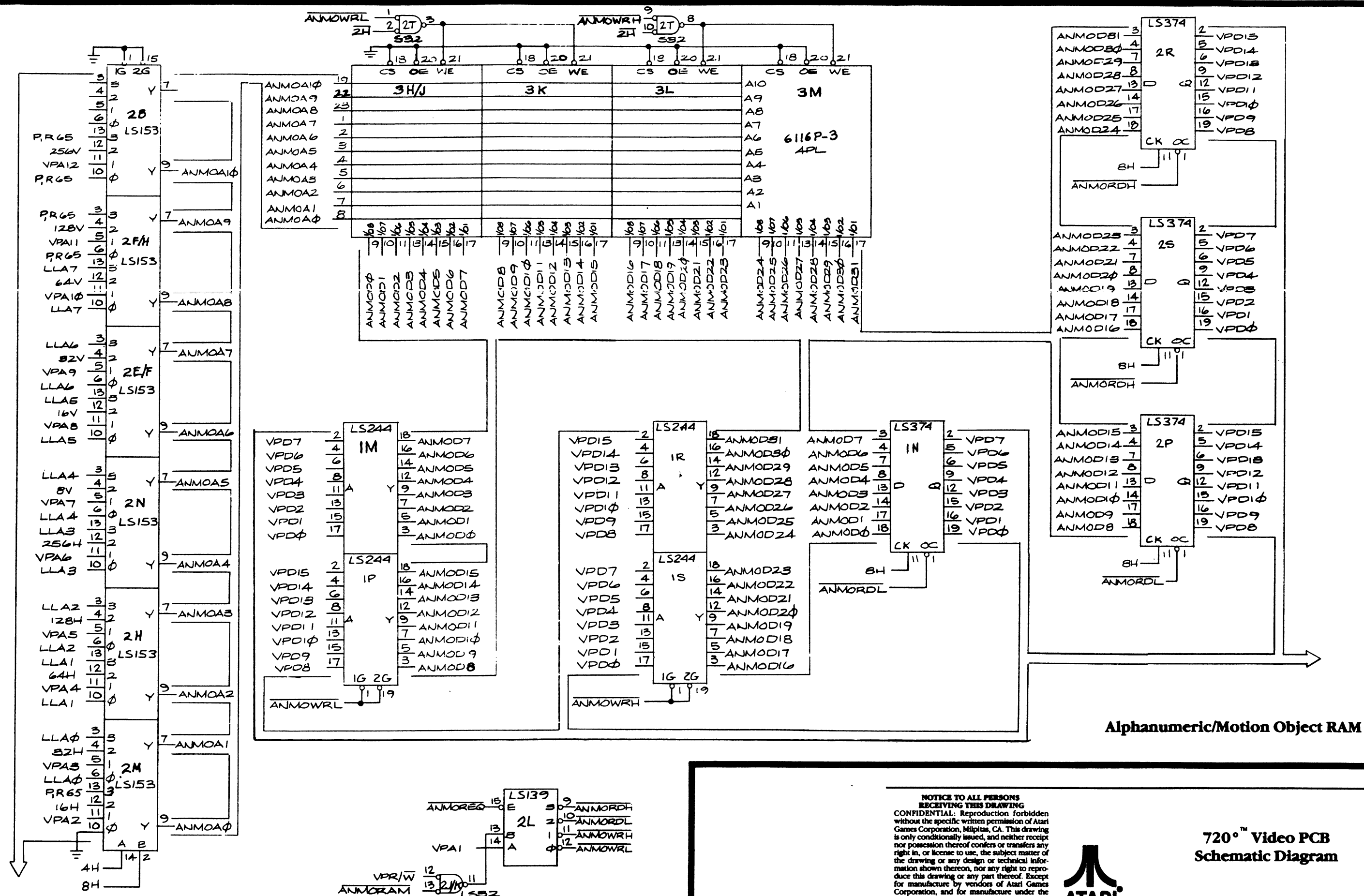
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720°™ Video PCB Schematic Diagram

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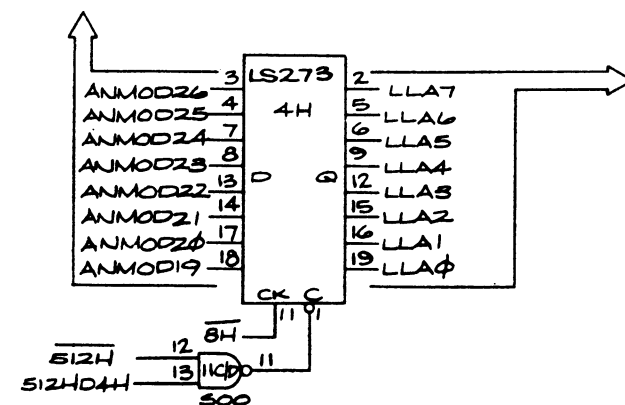
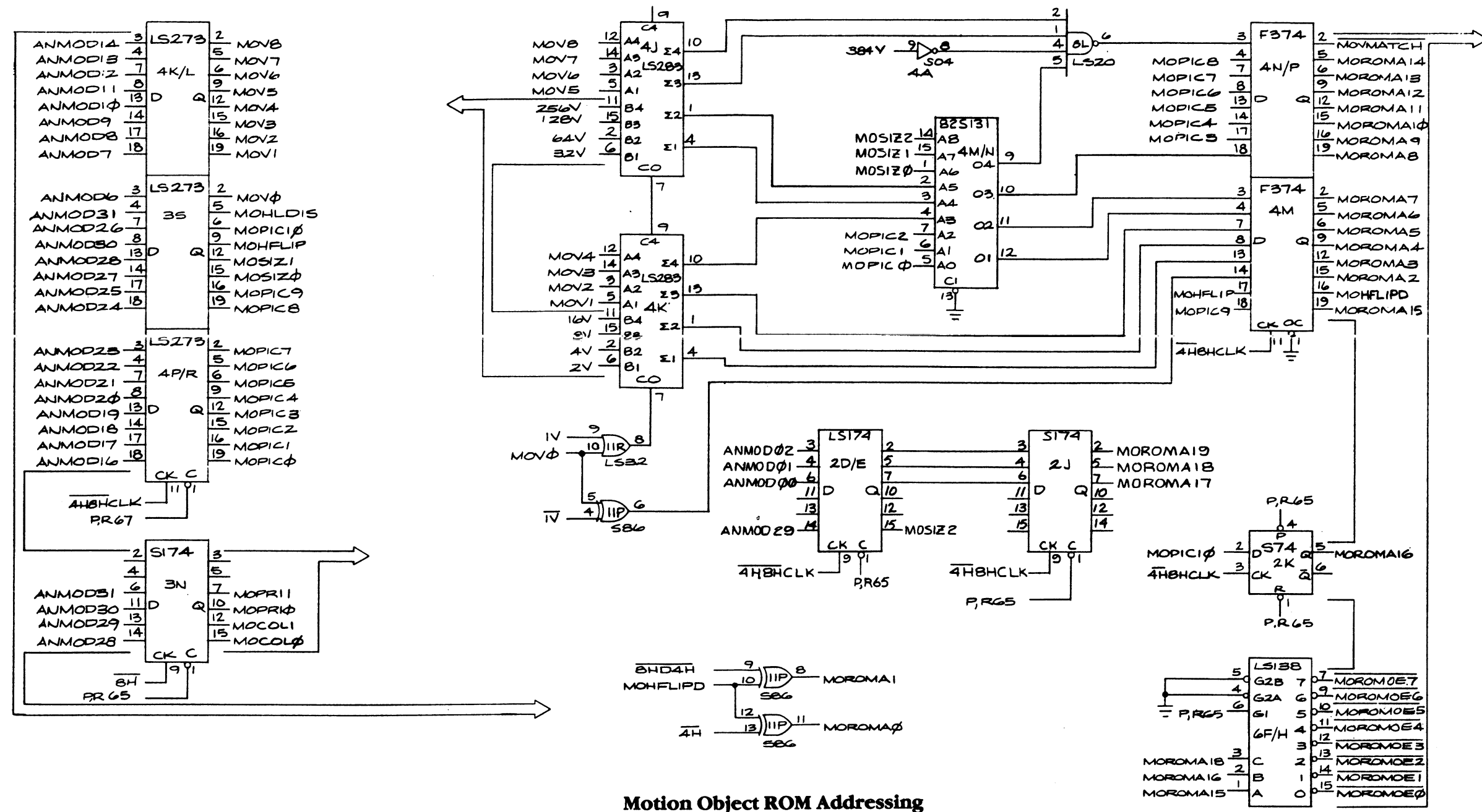
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720° Video PCB Schematic Diagram



Link List Address Latch

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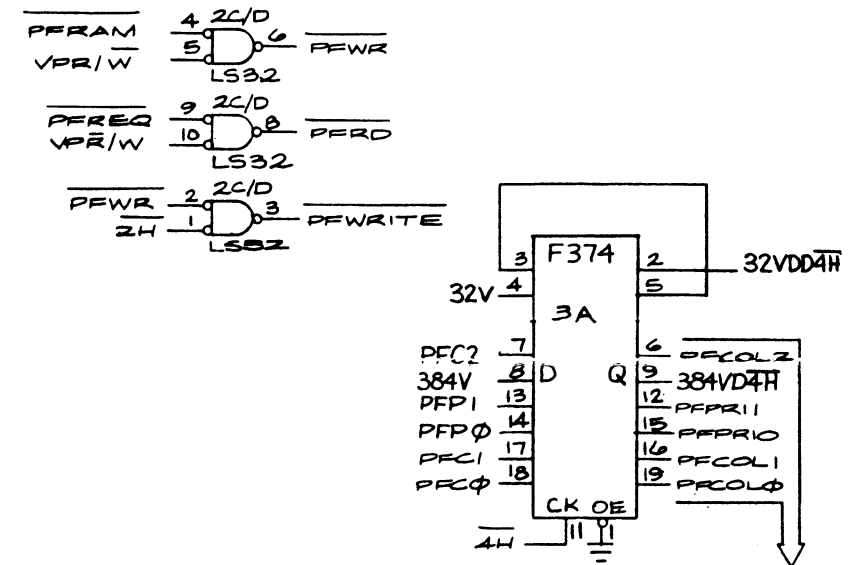
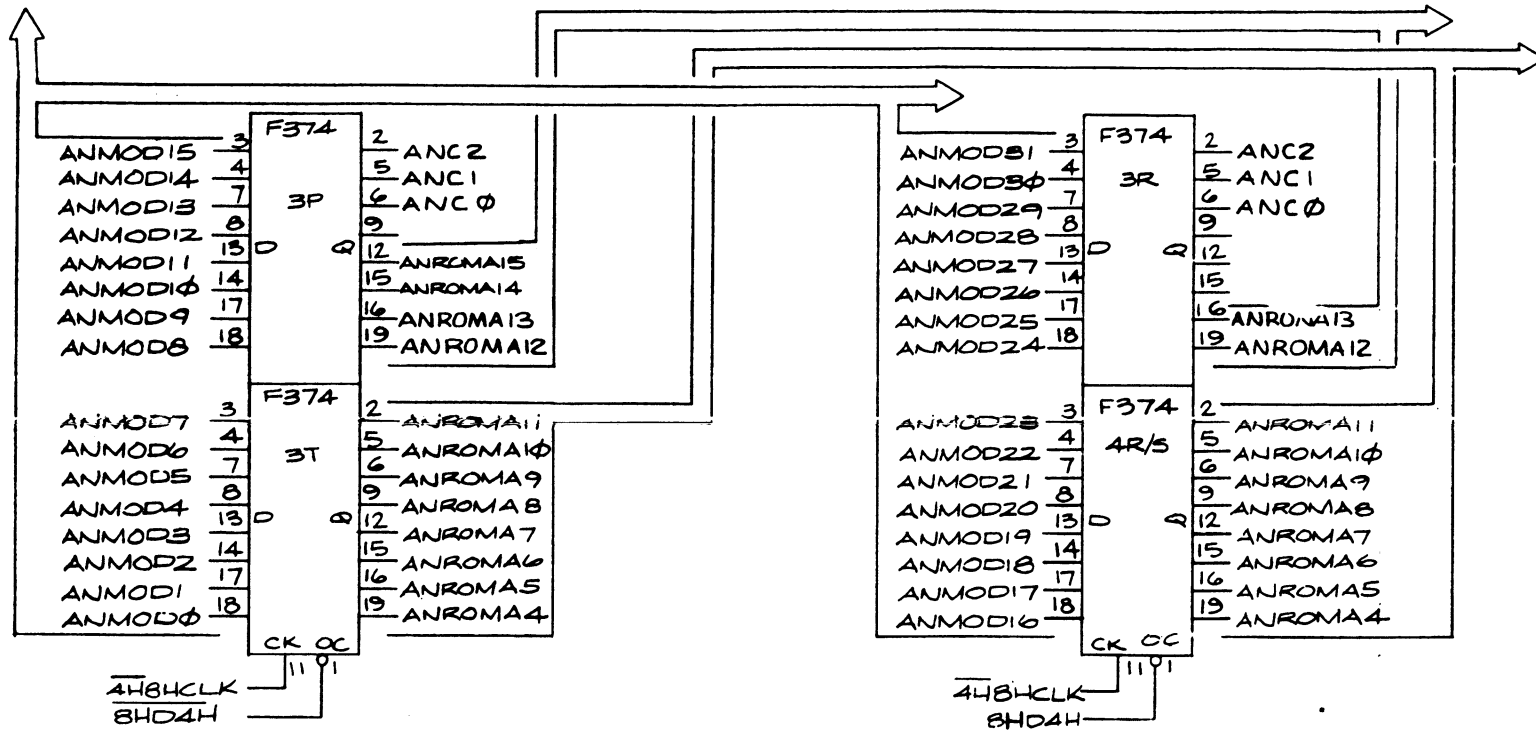


720°™ Video PCB Schematic Diagram

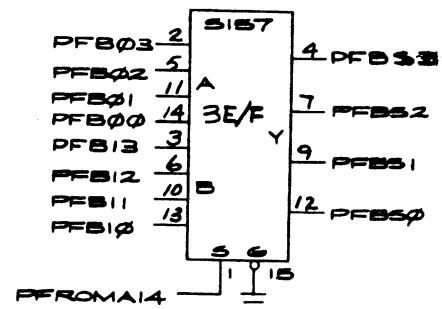
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Alphanumeric ROM Addressing



Playfield Data Latch Strobes



Playfield Bank Select

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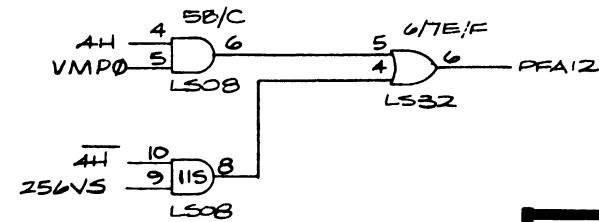


720°™ Video PCB Schematic Diagram

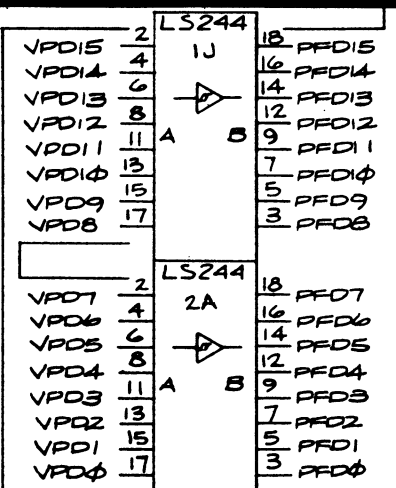
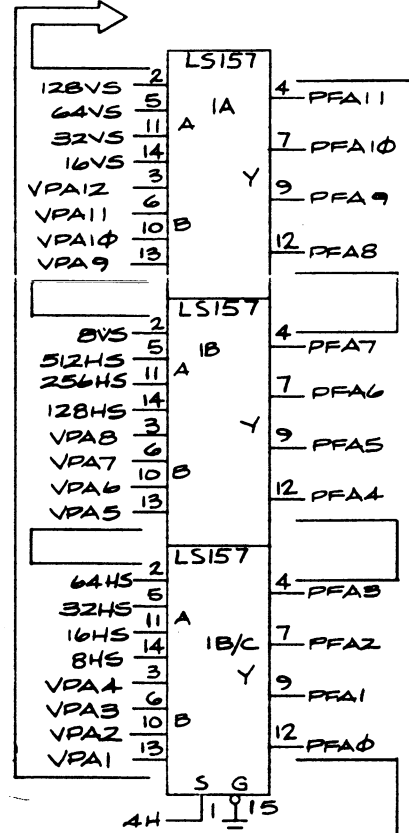
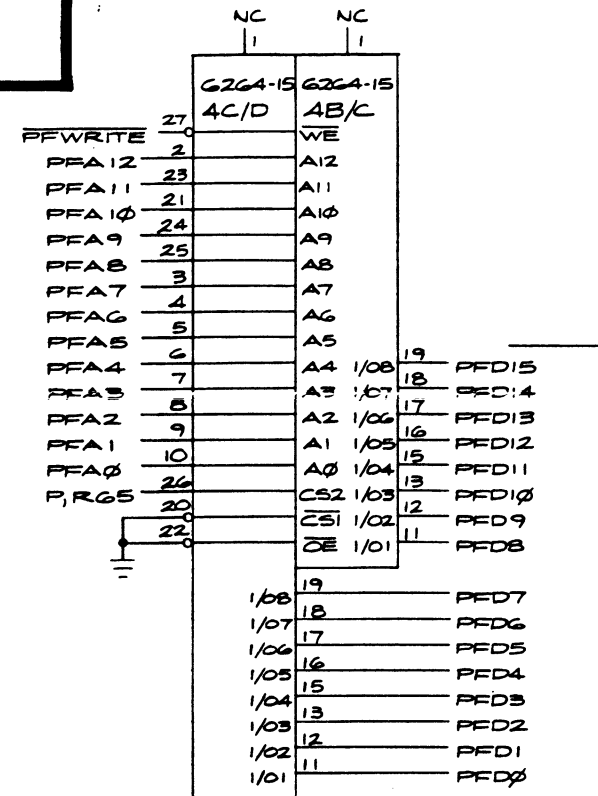
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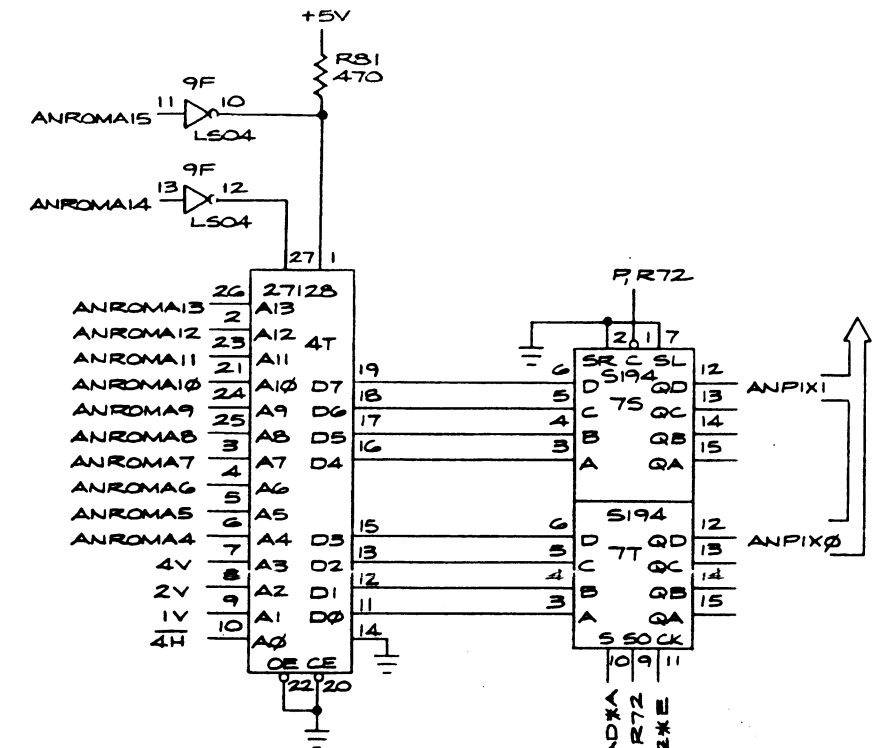
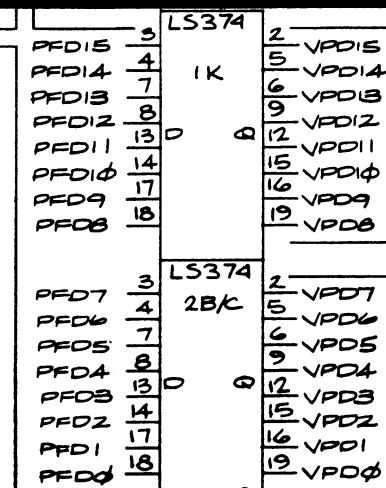
Playfield RAM Addressing



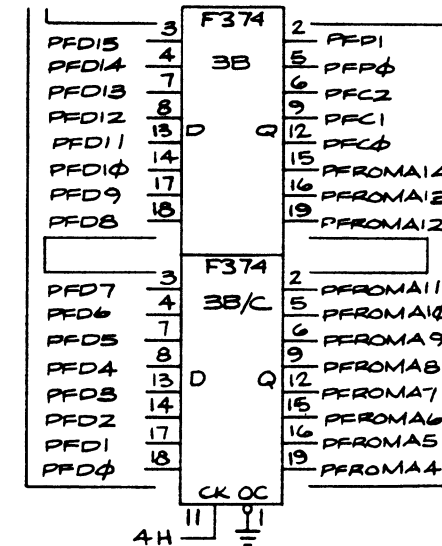
Playfield RAM



Playfield RAM Data Latches



Alphanumeric ROM



Playfield ROM Addressing

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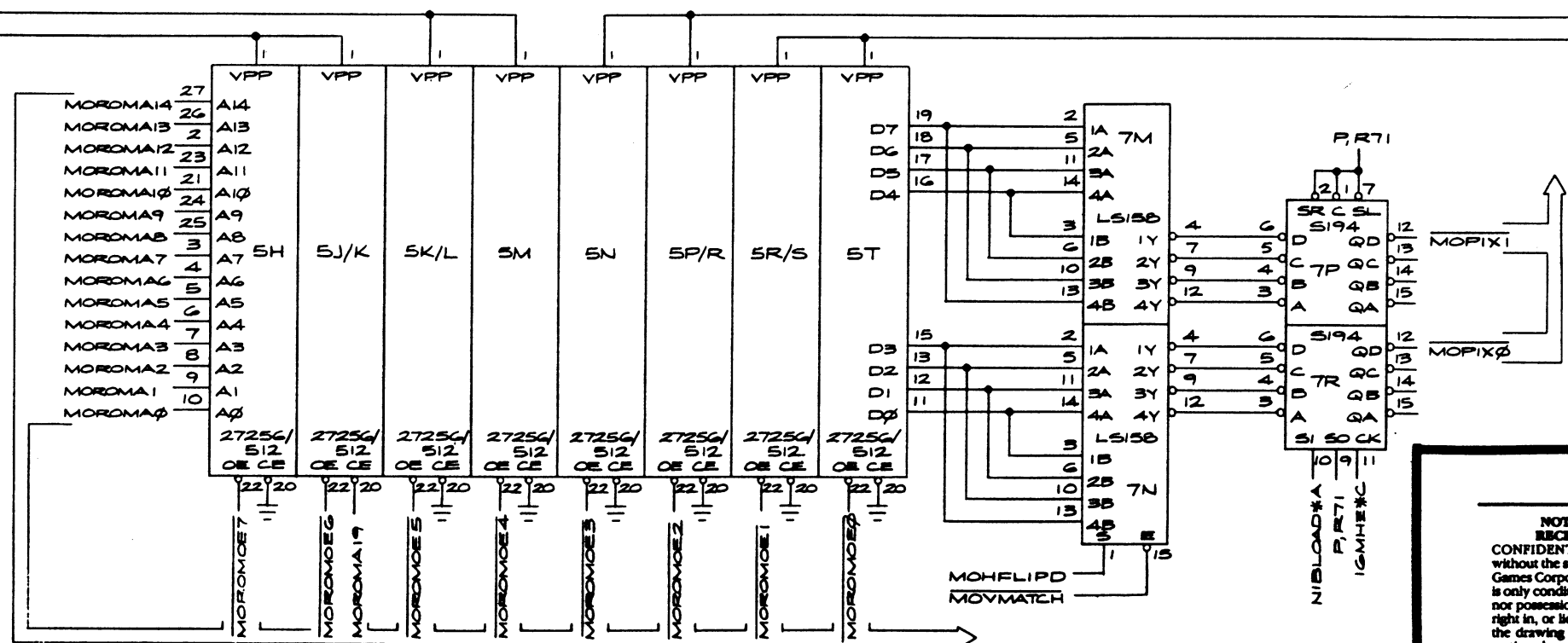
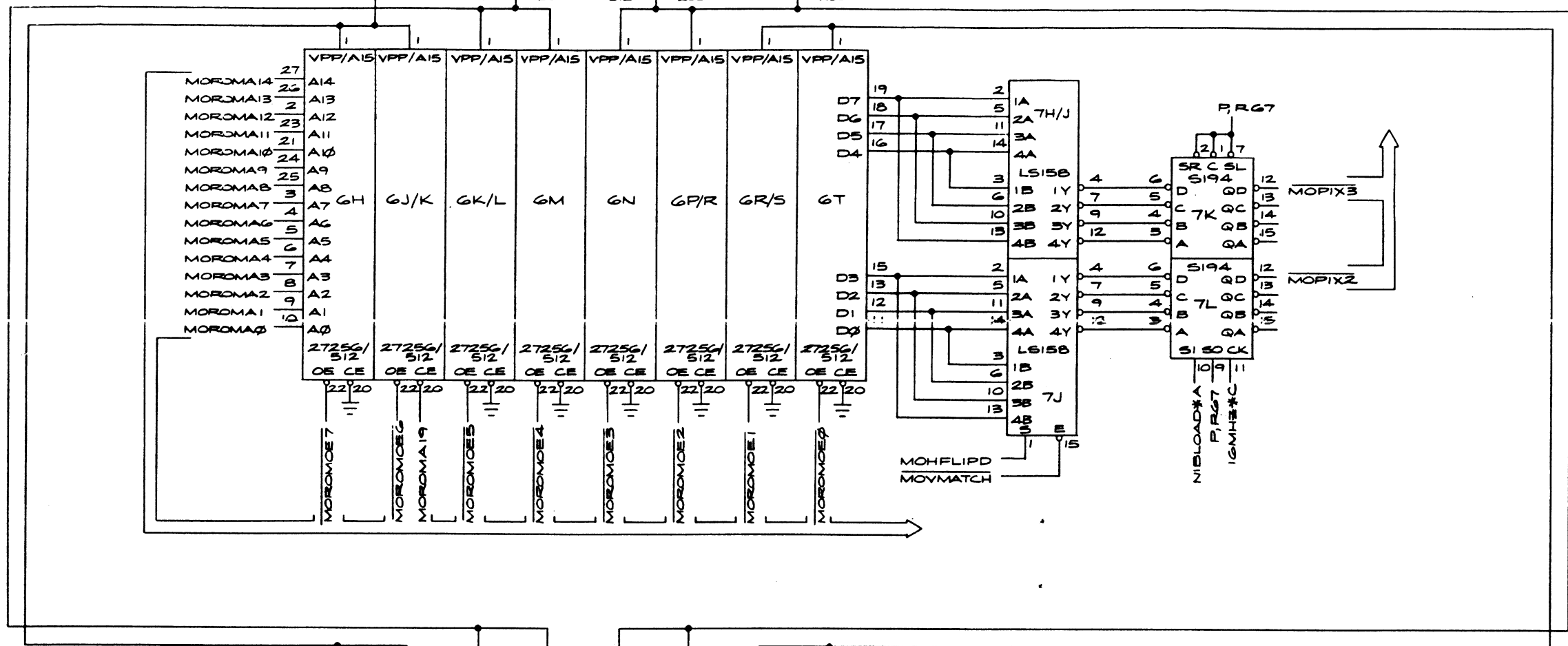


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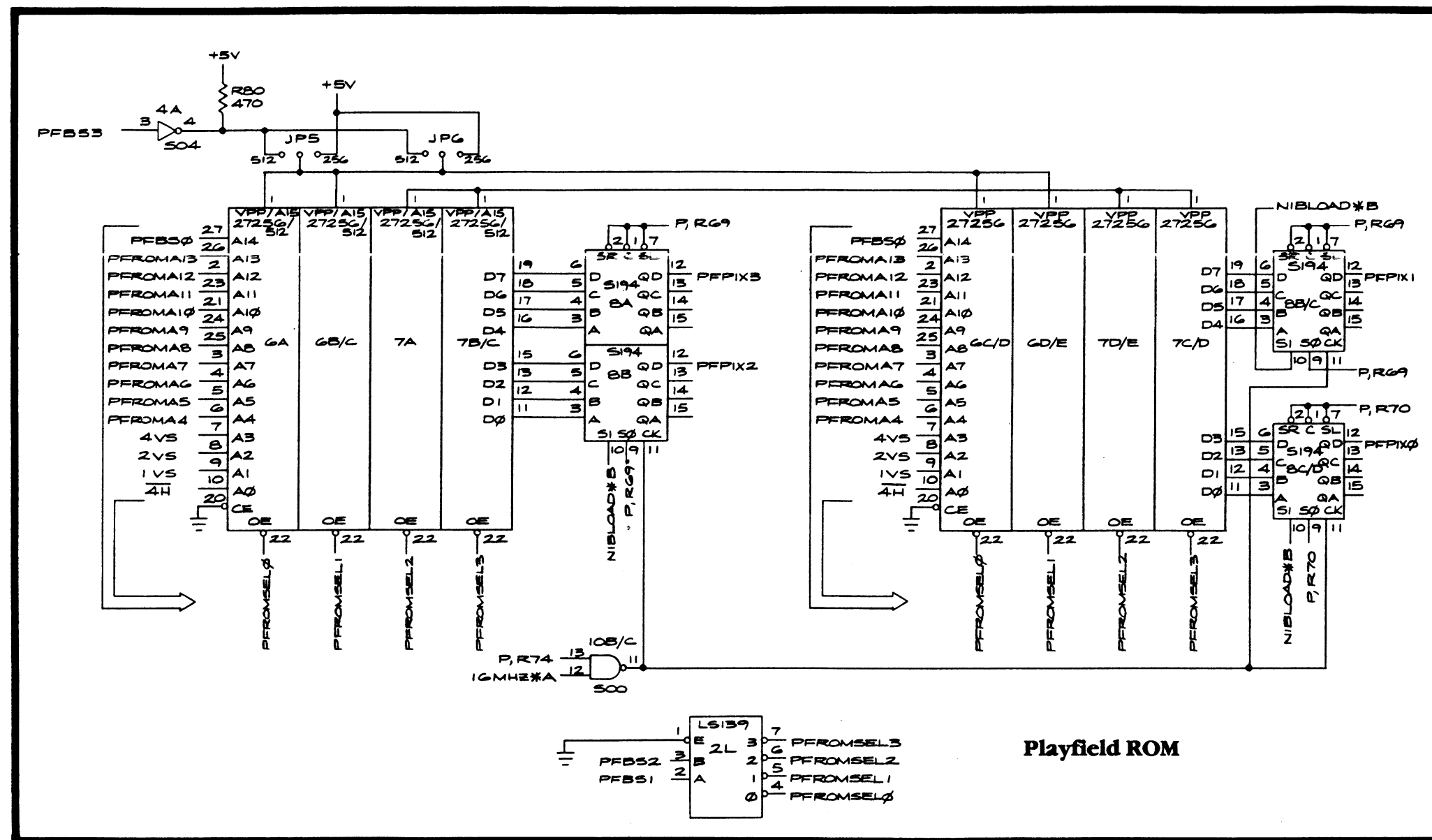
Motion Object ROM



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 Schematic Diagram



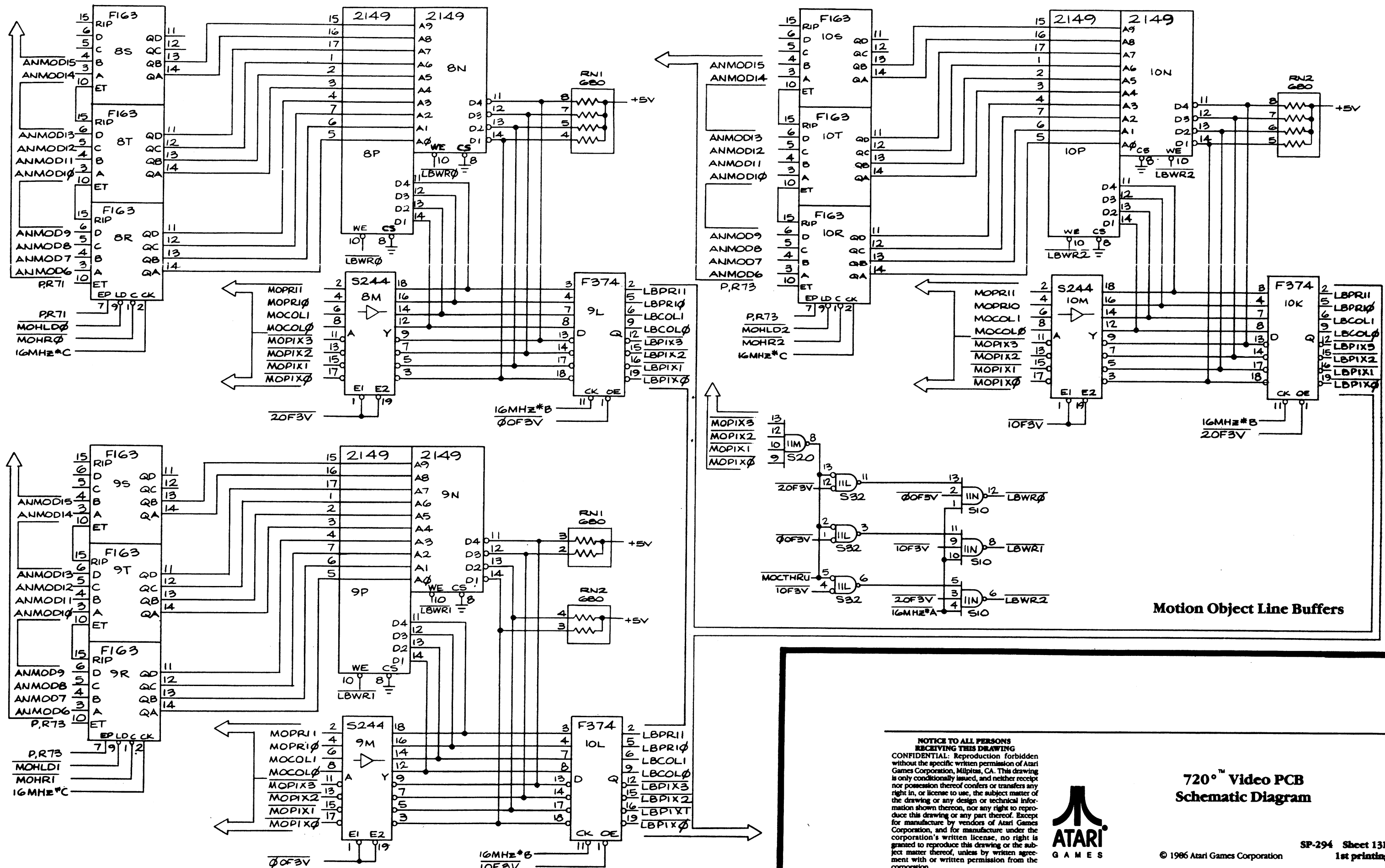
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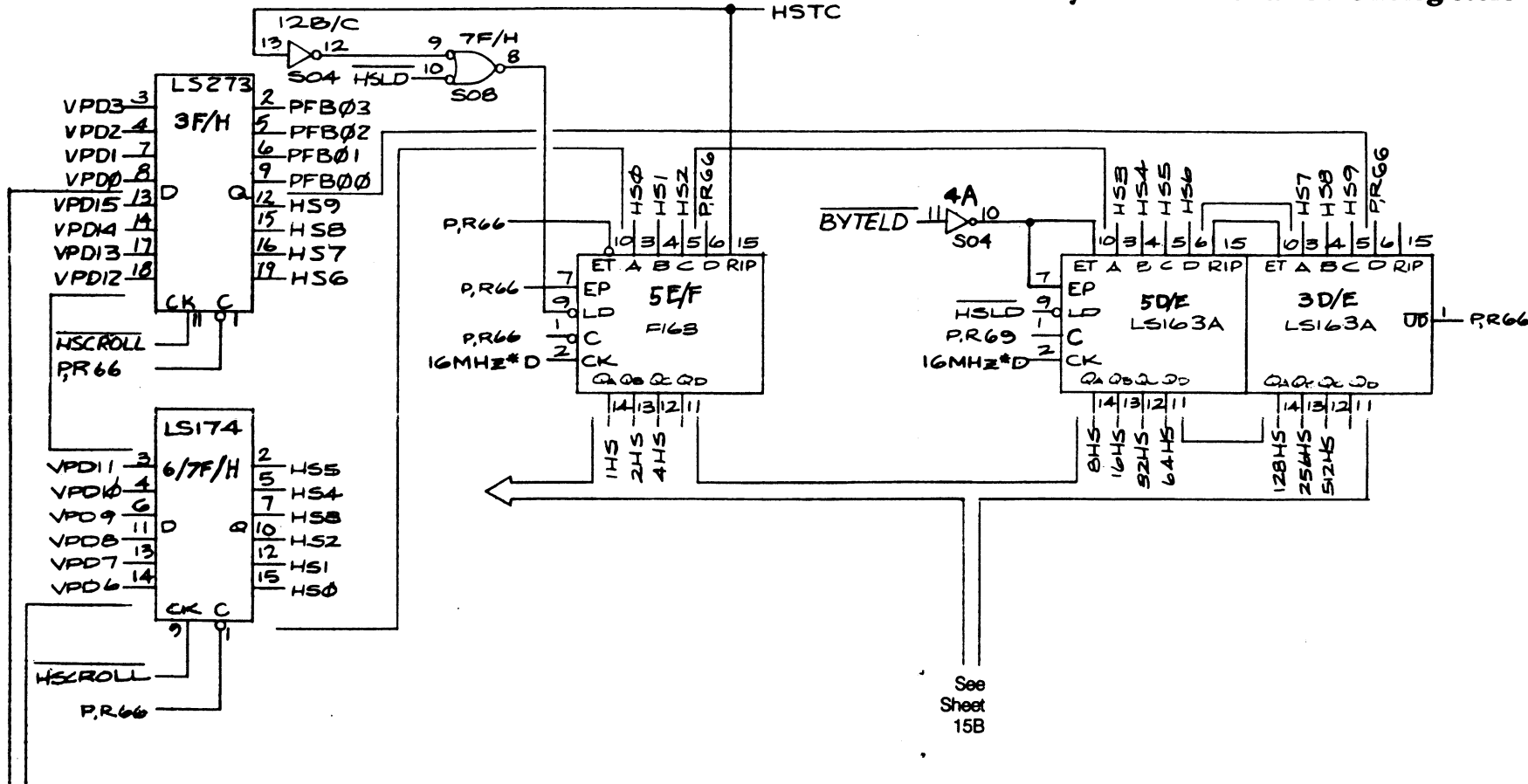


720° Video PCB Schematic Diagram

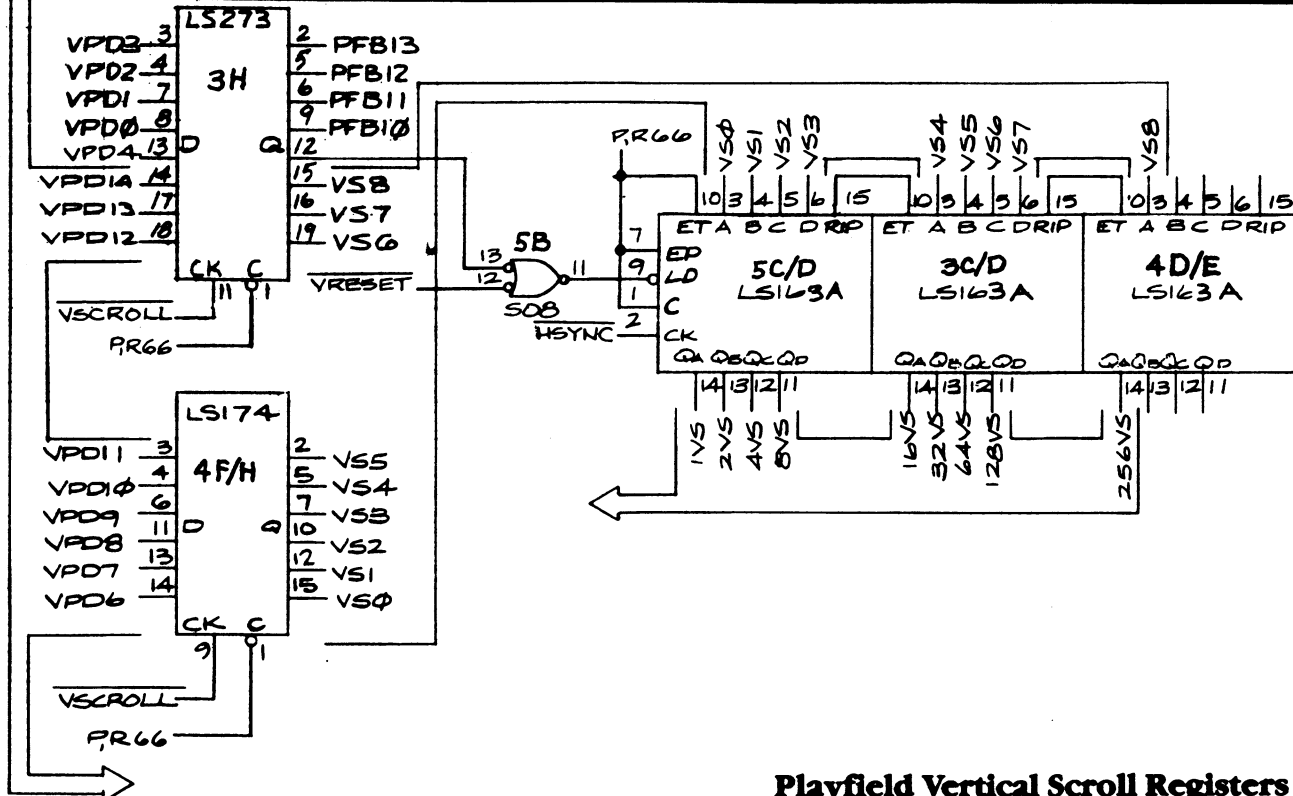
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Playfield Horizontal Scroll Registers



Playfield Vertical Scroll Registers



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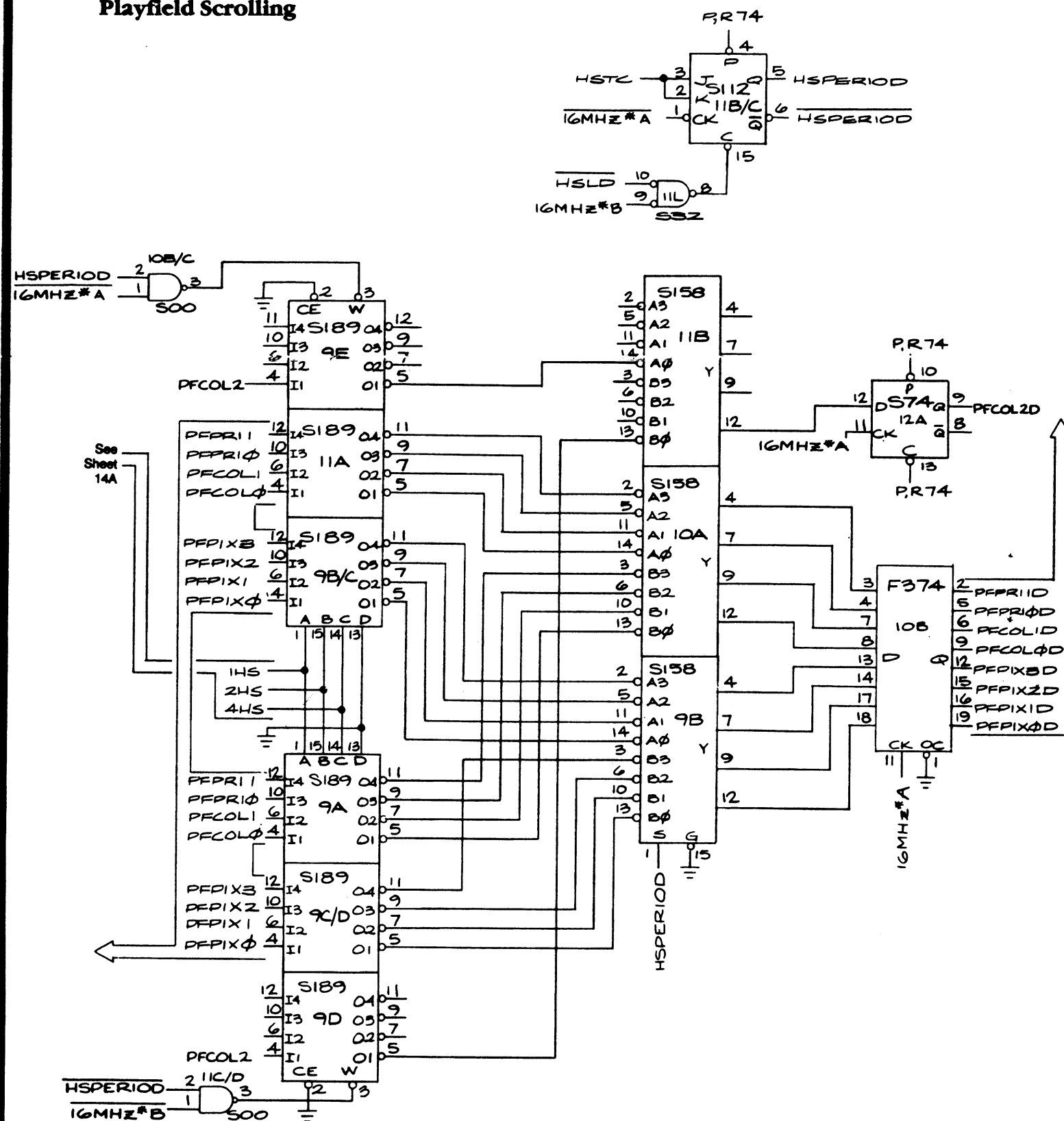
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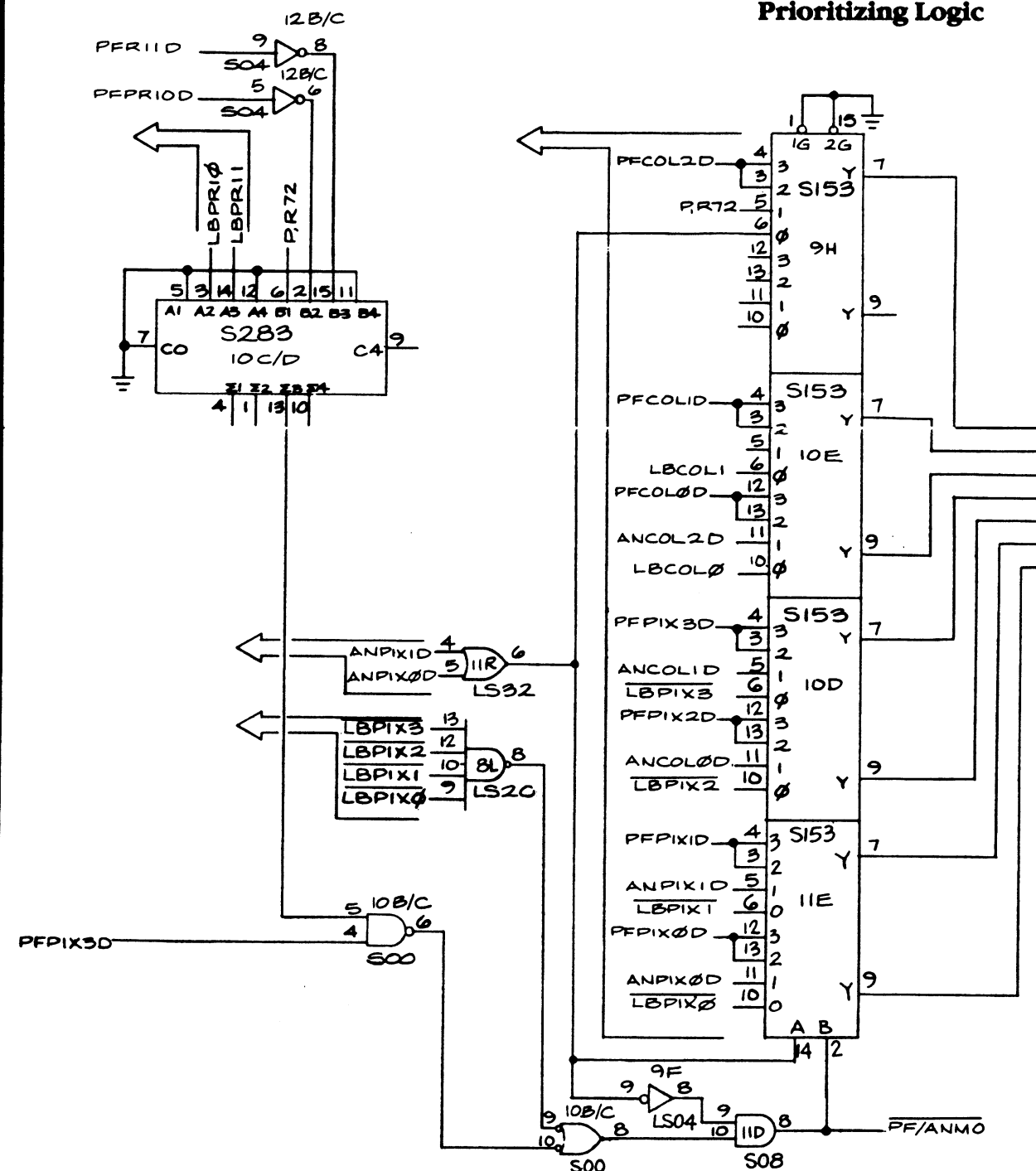
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Playfield Scrolling



Prioritizing Logic



Continued on Sheet 15A

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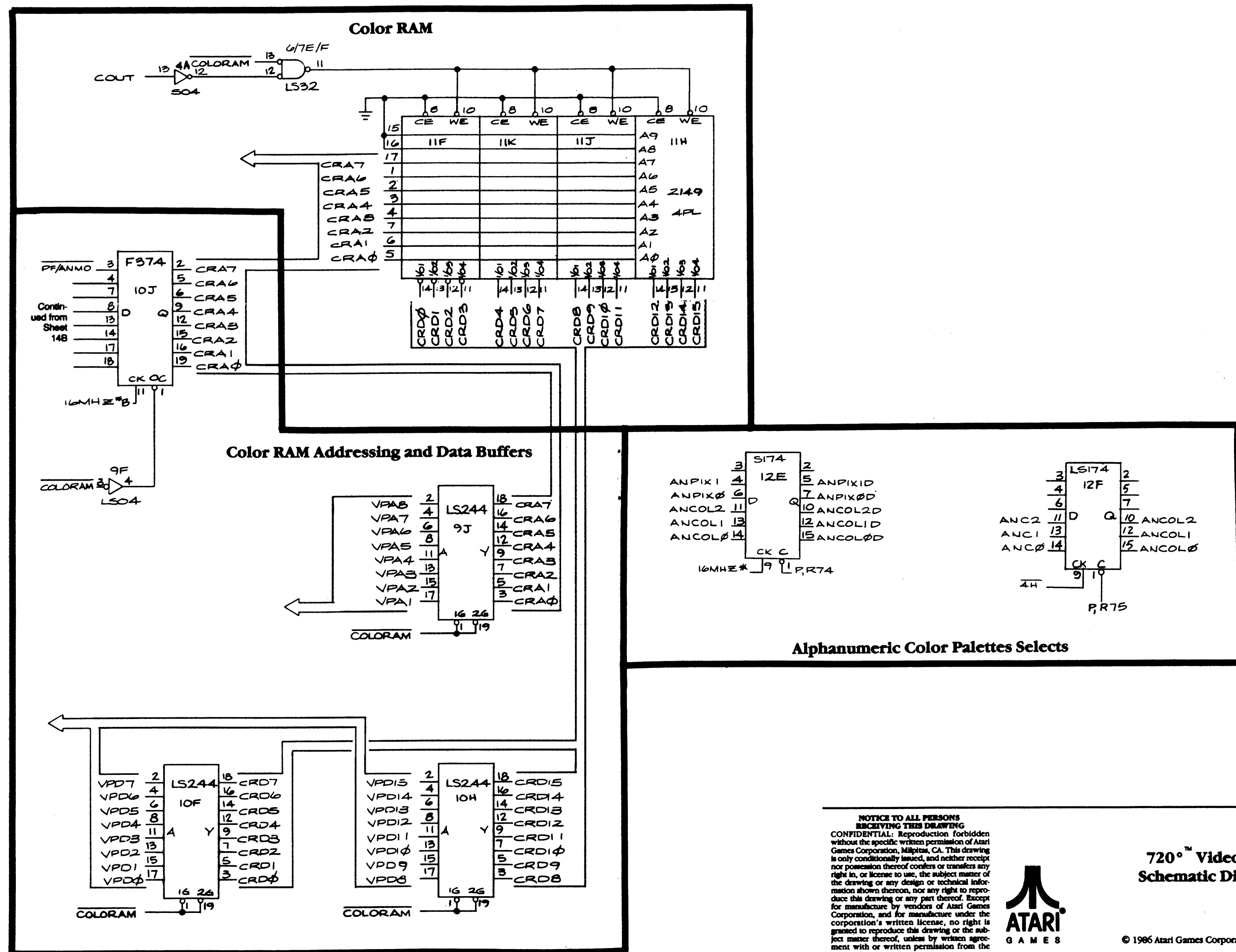
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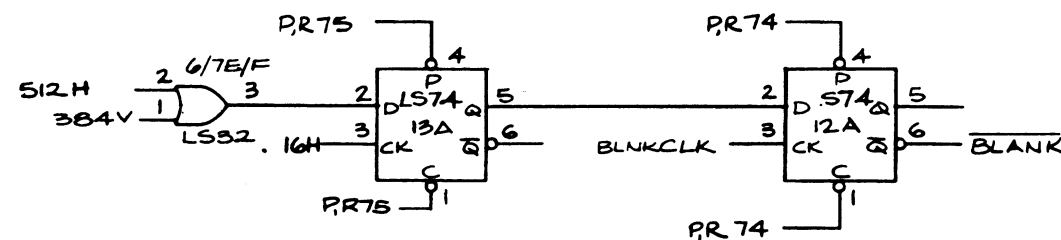
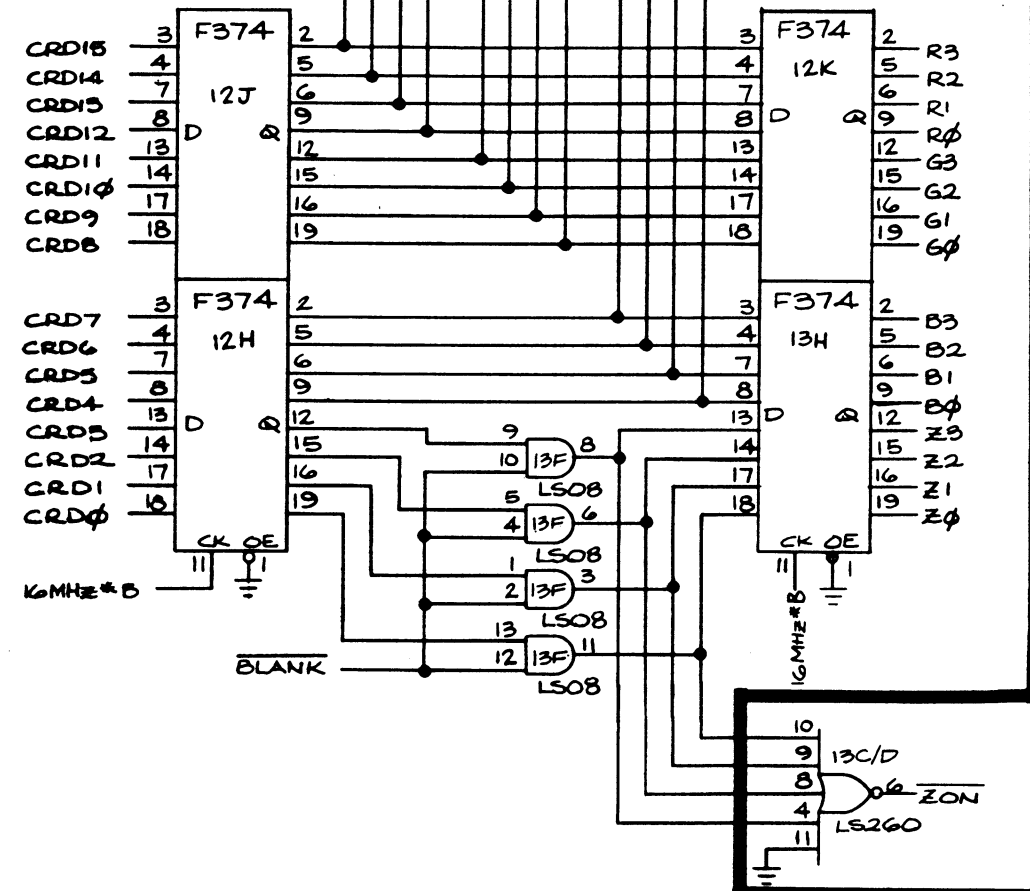
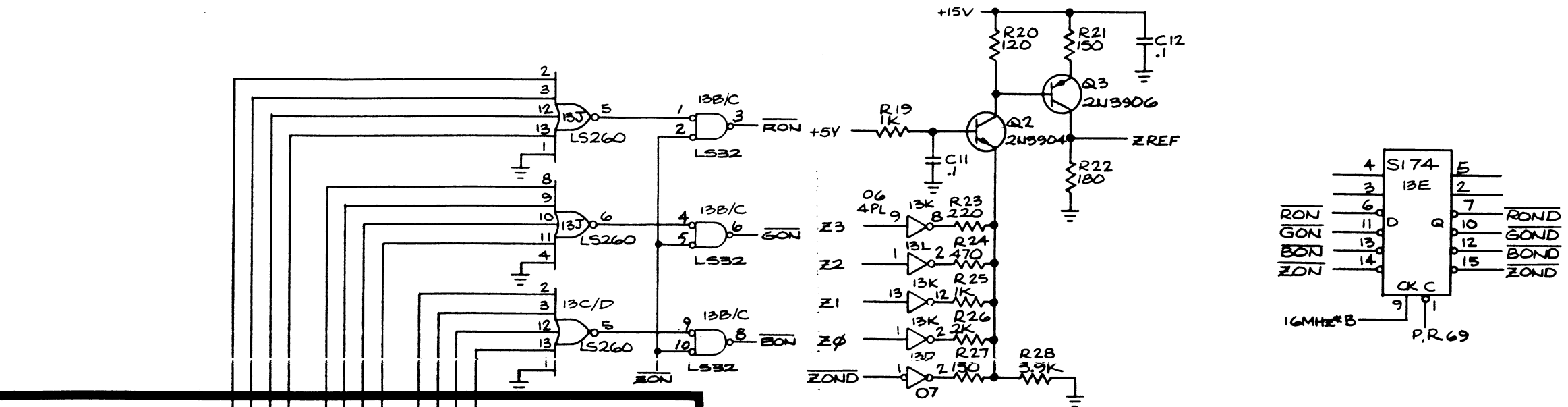


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**720°™ Video PCB
Schematic Diagram**

Video Intensity Control and Driver Enables



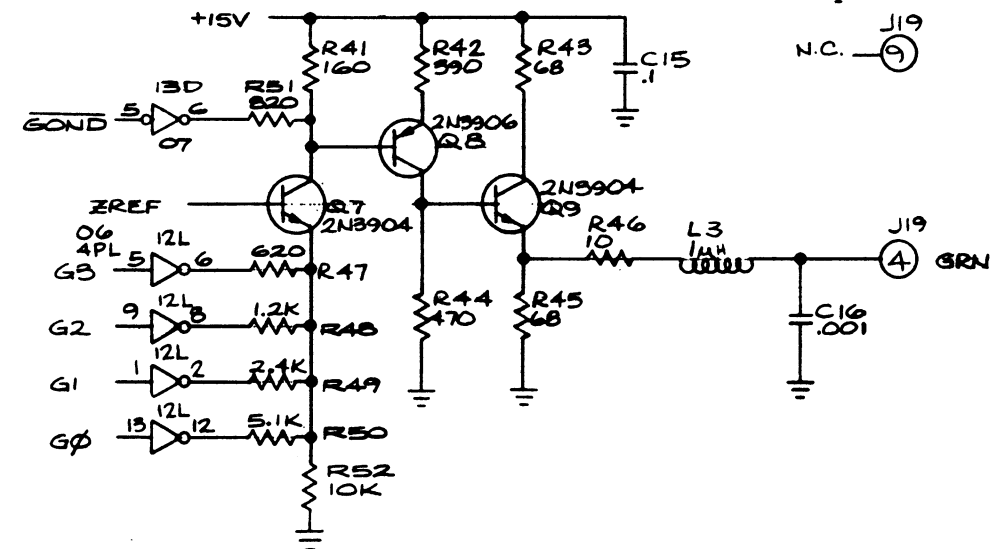
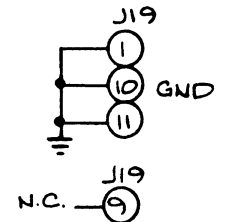
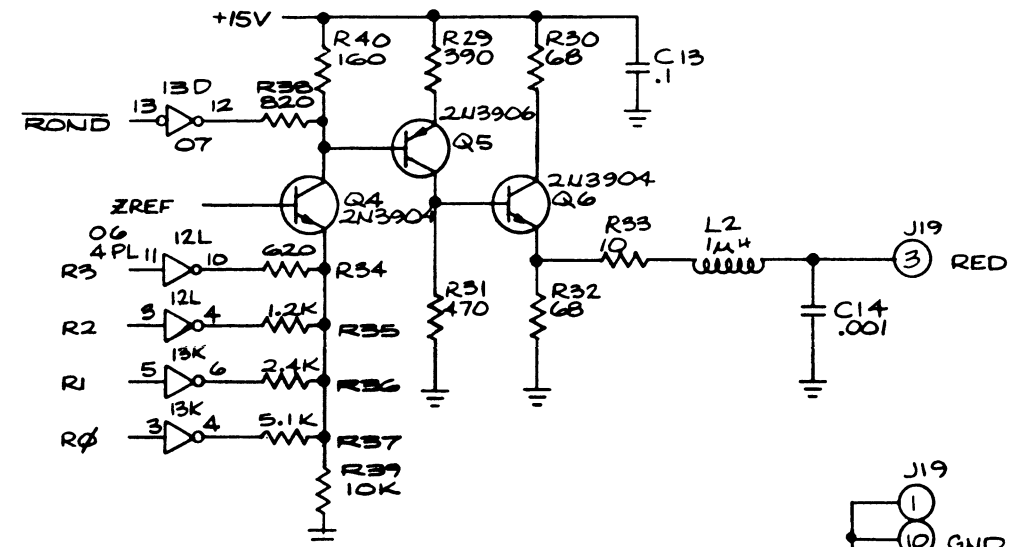
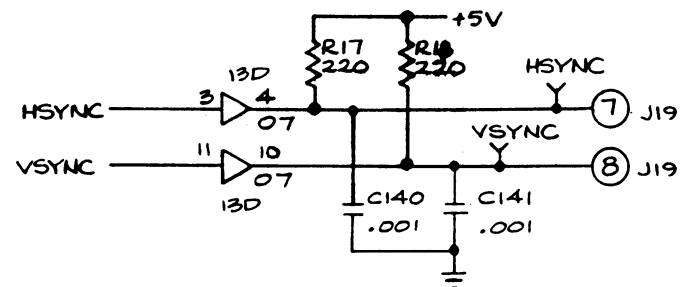
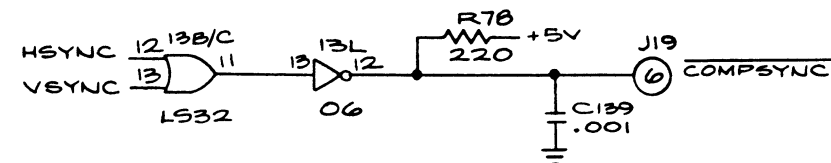
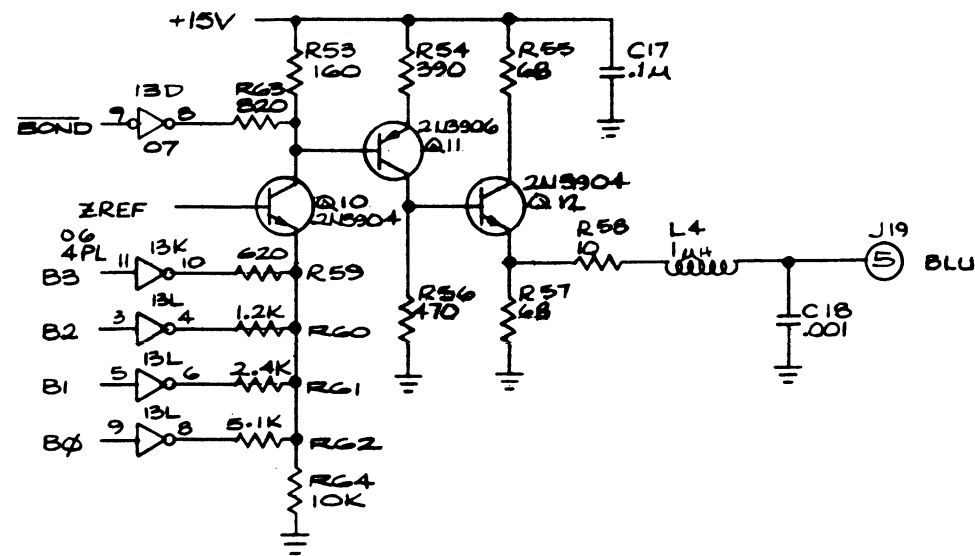
Data Latches and Blanking

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720° Video PCB Schematic Diagram

Output Drivers



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