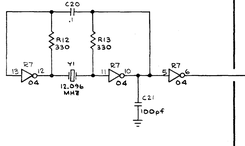
CLOCK



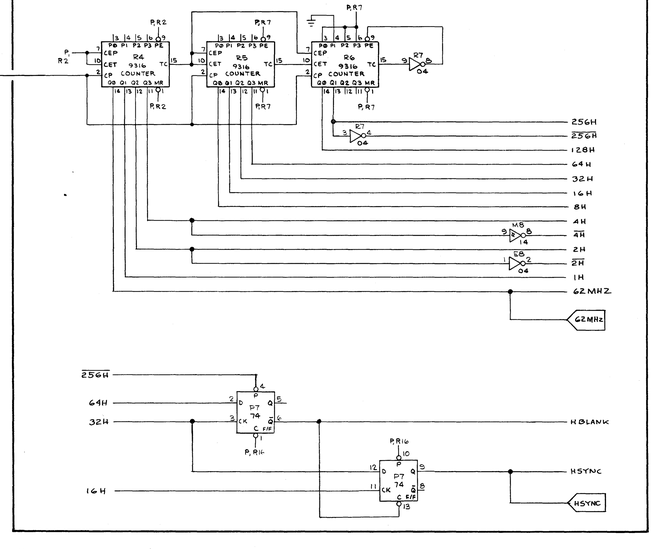
The basic frequency of the sync generator is a 12.096 MHz clock, generated by crystal Y1. The output of the oscillator, viewed with an oscilloscope, is a signal with a period of 83 nanoseconds.

The oscillator frequency is divided down by binary counters R4, R5, and R6. These provide various horizontal synchronization frequencies (1H thru 256H). The final output of the horizontal counting chain is 256H. This signal is, in effect, a division of the oscillator frequency by 768, or 15,750 Hz. The period of 256H is about 63.5 microseconds. The 256H signal, as well as other horizontal signals, are used to generate H BLANK and H SYNC timing pulses.

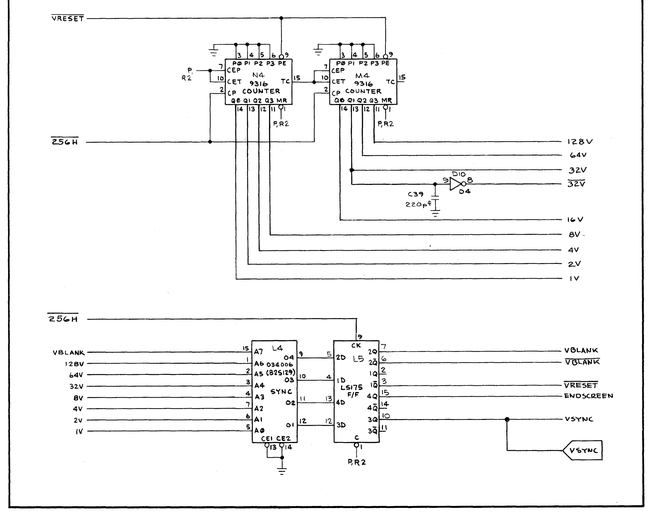
The $\overline{256H}$ signal is used to generate vertical sync signals 1V thru 128V. The 128V signal is, in effect, a division of the $\overline{256H}$ frequency by 262. This results in the final output from the counters of 60 Hz (16.6 milliseconds). The various vertical sync signals address sync PROM L4 whose data is latched at the output of L5.

The end result of the horizontal and vertical timing waveform is to synchronize the TV monitor display. This display consists of 262 horizontal lines per frame: only 240 lines are visible, since the last 22 lines occur during vertical blanking. Each line is equivalent to 768 clock pulses. Each frame is repeated 60 times per second, providing the necessary frequency of display refresh for a stable, non-flickering display.

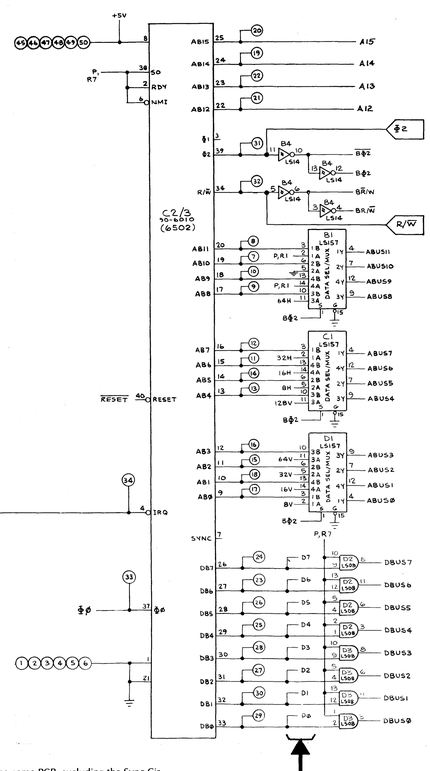
HORIZONTAL SYNC



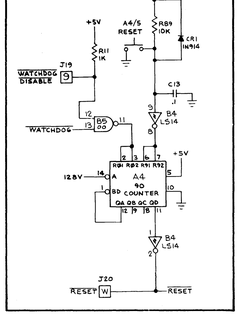
VERTICAL SYNC



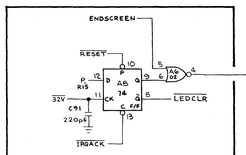
MICROPROCESSOR



WATCHDOG & POWER RESET



INTERRUPT REQUEST



The microprocessor controls all circuits on the game PCB, excluding the Sync Circuit and Watchdog and Power Reset Circuit. The Sync Circuit provides 4H (750 KHz) for the $\Phi 0$ clock input to the microprocessor.

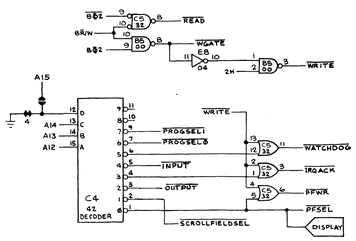
The Watchdog and Power Reset Circuit forces the microprocessor into its initilization sequence during intial power-up, or if the program strays from its normal sequence. When power is initially applied to the PCB, capacitor C13 and resistor R89 form a time constant that forces $\overline{RESET}$ low until the +5 VDC logic power becomes stable.

During normal operation, the microprocessor outputs address 5000 (hexadecimal) that is decoded by the address decoder for the $\overline{WATCHDOG}$ signal. This signal is received at the pin 13 input of B5. This signal input causes pins 2 and 3 of counter A4 to go high which resets the counter to a zero count output. If the $\overline{WATCHDOG}$ pulse is not received before the counter reaches the count of eight, $\overline{RESET}$ goes low, causing the microprocessor to jump to its initialization sequence.

Flip-flop A8 provides an interrupt request (IRQ) input to the microprocessor. The IRQ is a timing signal used by the microprocessor so it knows when to look for coins, when to write to the LED latches, and when to display motion objects.

Address bus ABUS0 thru ABUS11 is selected from either address lines AB0 thru AB11 from the microprocessor, or from various horizontal and vertical sync signals. This arrangement makes it possible for the microprocessor to write data into or read data out of the RAM when $B\Phi 2$ is high. When $B\Phi 2$ is low, data is read out of the RAM by the alphanumerics generator.

ADDRESS DECODER



The address decoder receives addresses from the microprocessor, decodes the addresses, and turns on the required circuitry for carrying out the instruction for that address. The address map, to the right of this text, is for the 4-Player Football game. This map provides the necessary information for operating the circuitry with the Atari Automatic ROM/RAM Tester. Before connecting the Tester, do the following:

1. Remove the microprocessor.
2. Short pin 37 to 39 of microprocessor socket C2/3.
3. Ground pin 9 of edge-connector J19.

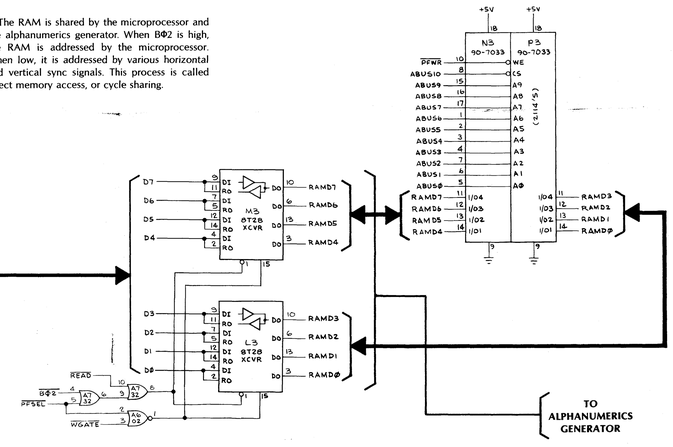
The ones and zeros in the ADDRESS column of the address map indicate the address necessary for information to be passed to and from the microprocessor. A 0 indicates that the address line is low, and a 1 indicates the line is high. Blank spaces indicate that it doesn't matter whether the address line is low or high. An A indicates that the address line is used as part of the functional address for that particular peripheral access. In the DATA column, a D indicates that the data line is used to transfer information.

MEMORY MAP

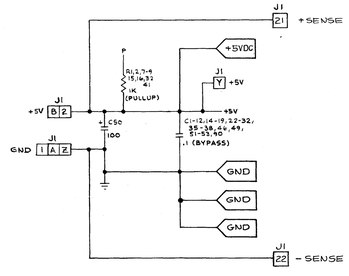
ADDRESS HEX	ADDRESS DEC	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF		X	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	X	D	D	D	D	D	D	D	0000-03FF WORKING RAM
																										0300-03FF FILD RAM & MOT OBJECTS
																										MOTION RAM ORGANIZATION
																										13C0 MOT OBJ 1 PIC NO.
																										13C1 MOT OBJ 1 VERT POS
																										13E0 MOT OBJ 1 HORZ POS
																										13E1 SPARE
																										13C2 MOT OBJ 2 PIC NO.
																										13C3 MOT OBJ 3 VERT POS
																										13E2 MOT OBJ 2 HORZ POS
																										13E3 SPARE
																										13D0 MOT OBJ 16 PIC NO.
																										13D1 MOT OBJ 16 VERT POS
																										13F0 MOT OBJ 16 HORZ POS
																										13F1 SPARE
0800-13FF		X	0	0	1	X	X	A	A	A	A	A	A	A	A	A	A	X	D	D	D	D	D	D	D	SCROLLFIELD
2000		X	0	1	0	X	X	X	X	X	X	X	X	X	0	0	W	D	D	D	D	D	D	D	D	SCROLLFIELD OFFSET
2001		X	0	1	0	X	X	X	X	X	X	X	X	0	1	W	X	X	X	X	X	X	D	D	D	WHISTLE SOUND
																		X	X	X	X	X	X	D	D	HIT SOUND
																		X	X	X	X	X	D	X	X	KICKER (RESETS NOISE GEN)
																		X	X	X	X	X	D	X	X	LD1
																		X	X	X	X	X	X	X	X	LD2
																		X	X	X	X	X	X	X	X	COIN CNTR LEFT
2002		X	0	1	0	X	X	X	X	X	X	X	X	X	1	0	W	X	X	X	X	X	D	D	D	CROWD AMP
																		X	X	X	X	D	X	X	X	COIN CNTR RIGHT
																		X	X	X	X	X	X	X	X	ATTRACT
2003		X	0	1	0	X	X	X	X	X	X	X	X	X	1	1	W	X	X	X	X	D	D	D	D	LED DRIVERS
3000		X	0	1	1	X	X	X	X	X	X	X	X	X	X	X	W	X	X	X	X	X	X	X	X	COIN CNTR CENTER
																		X	X	X	X	X	X	X	X	TRACK (CLEARS IRQ LATCH)
4000		X	1	0	0	X	X	X	X	X	X	X	X	X	0	0	R	D	D	D	D	D	D	D	D	(LD1 & LD2 LO) TRACK BALL DIR
																		D	D	D	D	D	D	D	D	(LD1 HI & LD2 LO) RIGHT PLAYER TEAM 1 TRACK BALL CNTRS
																		D	D	D	D	D	D	D	D	(LD1 & LD2 HI) LEFT PLAYER TEAM 2 TRACK BALL CNTRS
4001		X	1	0	0	X	X	X	X	X	X	X	X	X	0	1	R	D	X	X	X	X	X	X	X	ENDSCREEN
																		X	X	X	X	X	X	X	X	TEST
																		X	X	X	X	X	X	X	X	COIN 2
																								D	D	COIN 1
4002		X	1	0	0	X	X	X	X	X	X	X	X	X	1	0	R	D	X	X	X	X	X	X	X	(LD1 & LD2 LO) SEL1 7 4
																		D	D	X	X	X	X	X	X	(LD1 & LD2 HI) SEL2 6 5
																		A	X	D	X	X	X	X	X	(LD1 & LD2 LO) SLAM 5 6
																		A	X	X	X	X	X	X	X	(LD1 & LD2 HI) Z/APYSEL 4 7
																		X	X	X	X	D	D	D	D	DIP SW
																		D	D	D	D	D	D	D	D	(LD1 HI & LD2 LO) RIGHT PLAYER TEAM 2 TRACK BALL CNTRS
																		D	D	D	D	D	D	D	D	(LD1 & LD2 HI) LEFT PLAYER TEAM 2 TRACK BALL CNTRS
5000		X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	W	X	X	X	X	X	X	X	X	WATCHDOG
6800-7FFF		X	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	PROGRAM

RANDOM-ACCESS MEMORY

The RAM is shared by the microprocessor and the alphanumerics generator. When $B\Phi 2$ is high, the RAM is addressed by the microprocessor. When low, it is addressed by various horizontal and vertical sync signals. This process is called direct memory access, or cycle sharing.



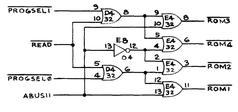
POWER INPUT

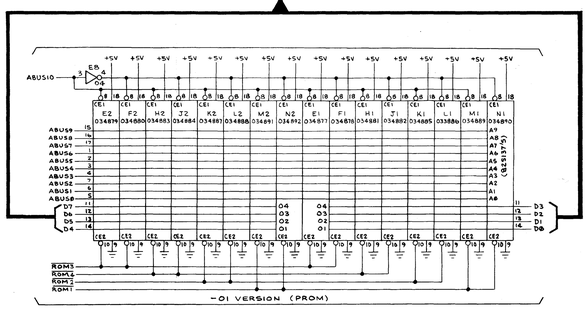


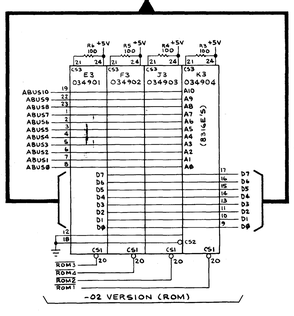
PROGRAM MEMORY

Your 4-Player Football game PCB may contain one of serveral possible program memory chips sets. The -01 version of the PCB contain 16 PROMs for the memory.

The -02 version contains 4 ROM chips for the memory. A third possiblity would be a mixture of ROMs and PROMs. For information regarding which ROMs are equivalent to which PROMs, see the Illustrated Parts Catalog chapter of the game manual.







denotes a test point

4-PLAYER FOOTBALL MICROCOMPUTER, CLOCK, SYNC AND MEMORY
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